PhD Vincenzo Terracciano

Modeling and Investigation of MPS & JBS Diodes and New Power Device Architectures

Tutor: Andrea Irace
Co-Tutor: Vincenzo d'Alessandro

Cycle:XXXVIII Year: Third

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My background

- MSc degree: *Electronic Engineering*
- Research laboratory: *OPTO-POWER LAB*
- PhD start date: *01/11/2022*
- Scholarship type: *ITEE*
- Partner company: *Vishay Semiconductor*

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SUMMARY OF PhD ACTIVITIES

Ad hoc PhD courses	Courses
❑ Numerical Methods For Thermal Analysis, Modeling, And simulation: Application to Electronic Devices And systems (DIETI)	❑ Numerical Models For The Fields(DIETI)
❑ Fiber Optic Sensing And Optoelectronic Circuits: Design And Application(DIETI)	❑ Analitycal Mechanics (Physics Dep.)
❑ Academic Entreprenuership (DIETI)	❑ Electrodynamics of Continuos Media (DIETI)
❑ How to boost your PhD (DIETI)	

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SUMMARY OF PhD ACTIVITIES

Contributions To Conferences	
International Conference on Silicon Carbide and Related Materials (ICSCRM), *Sorrento Italy 2023,*	*POSTER*
29th International Workshop on Thermal Investigations of ICs and Systems (THERMINIC), *Budapest Ungary* 2023.	ORAL
International Conference on Silicon Carbide and Related Materials (ICSCRM), *Raleigh USA 2024.*	✗
European Symposium on Reliability of Electron Devices, Failure Physics and Analysis (ESREF), *Parma Italy* 2024.	✗
31th International Workshop on Thermal Investigations of ICs and Systems (THERMINIC), *Napoli Italy* 2025.	ORAL
European Symposium on Reliability of Electron Devices, Failure Physics and Analysis (ESREF), *Bordeaux France* 2025.	ORAL

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SUMMARY OF PhD ACTIVITIES

THERMINIC 2025 ((31st INTERNATION
Thermal Investigati

BEST PAPER AWARD

VINCENZO TERRACCIAI

Department of Electrical Engineering and Information Technolo
University of Naples Federico II, Italy & Vishay Semiconductor, Turi

FOR THE CONTRIBUTION

Electrothermal Performance Enhancement of Silicon Carbide (
Around MOSFETs using a Ferroelectric Gate Stack

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SUMMARY OF PhD ACTIVITIES

PhD School

China-Italy Joint Laboratory on Advanced Manufacturing (CI-LAM)
Summer School Chair: **Prof. *Giovanni Breglio***

CI-LAM China - Italy Joint Laboratory on Advanced Manufacturing 中意先进制造联合实验室 | UNIVERSITÀ DEGLI STUDI DI BERGAMO | Università degli Studi di Napoli Federico II | 清华大学 Tsinghua University

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[1] Circuit Modelling Of SiC Merged PiN Schottky diodes

Objectives:

1. To realize a **compact scalable physically electro-thermal model** to describe and prevent the effect of **surge current** event in the **SiC Merged PiN Schottky** diode. The model must take into account the detrimental ***snapback*** mechanism.

2. The model should be more **useful and flexible** respect than standard electro-thermal TCAD simulation.

Methodology:

1. The effectiveness of the model is assessed through comparison with TCAD simulations.

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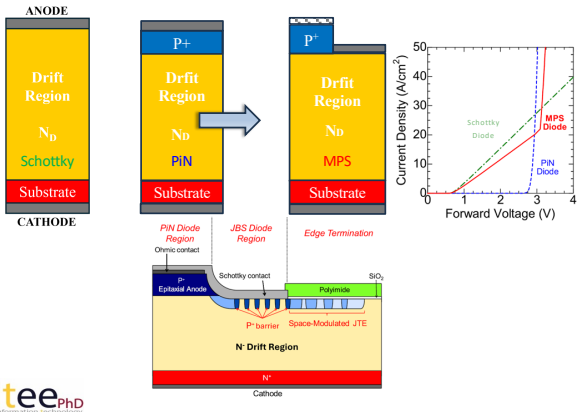
[1] Merged PiN Schottky: Structure



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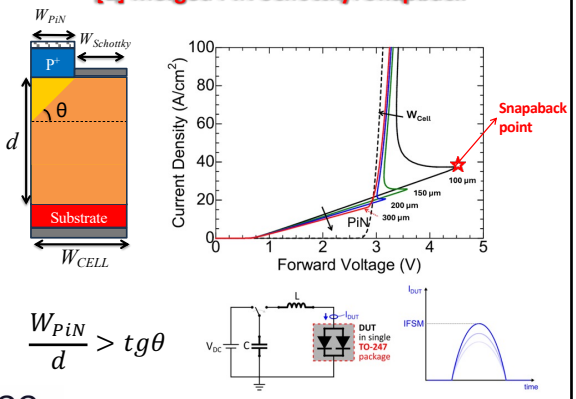
[1] Merged PiN Schottky: Snapback



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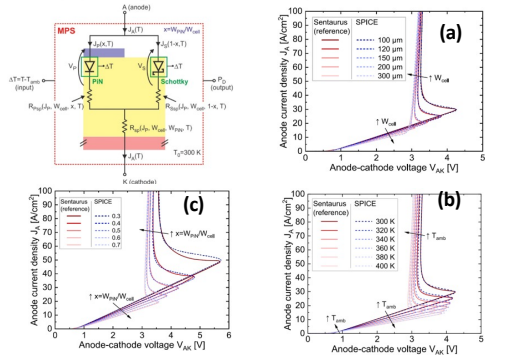
[1] Merged PiN Schottky: Circuit Model



(a) I-V Forward Curve by varying W_{CELL}, (b) by varying W_{PiN} keeping W_{CELL}=100 µm
(c) By varying temperature

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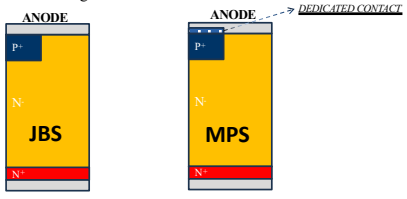
[1] Optimal bonding of 4H-SiC parallel diodes in a single TO-247 package for improved surge current robustness: experimental investigation

1. Proving how **an innovative stitch bond–wire configuration** can dramatically boost the ***surge current capability*** of 1200 V SiC JBS diodes.
2. Revealing the **distinctive failure mechanisms** associated with different bond–wire layouts investigated in this work.



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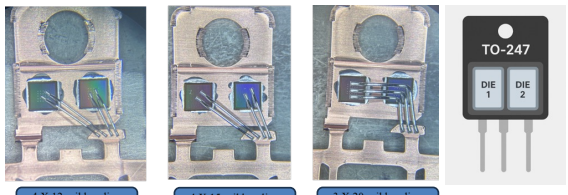
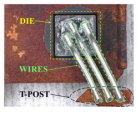
[1] Experiments



4 X 12 mil bonding wire | 4 X 15 mil bonding wire | 3 X 20 mil bonding wire (Stitch)

Three alternative bond wire configurations were implemented and tested. In the first two configurations, **the two 30 A dies are connected in parallel using four 12 mil and 15 mil bond wires**, where two wires directly connect the T-Post to each die. In the third configuration, three 20 mil bond wires are used to connect **one die to the other**, with **only one die being directly linked to the T-Post**.



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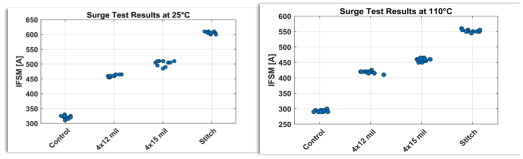
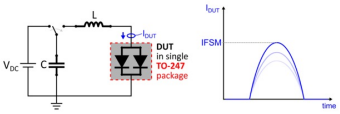
[1] Experimental Results



The DUTs were divided into two batches and subjected to surge current tests at **25 °C** and **110 °C**. Each device underwent consecutive surge pulses, with the **current amplitude increasing in 5 A** increments between tests.



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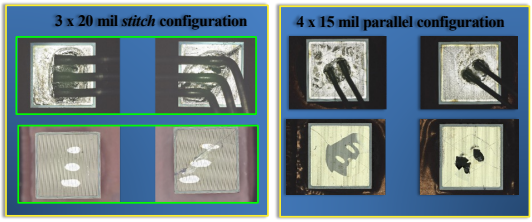
[1] Failure mechanism of stitch bond-wire configuration



The **stich** configuration shows a **asymmetrical failure** mechanism respect than the parallel configurations; In practice, the **stitch** configuration frequently **showed only the right die exhibiting visible cracks**, **while the left die remained intact**. In contrast, in the **parallel configurations, both dies were consistently cracked** after the surge test

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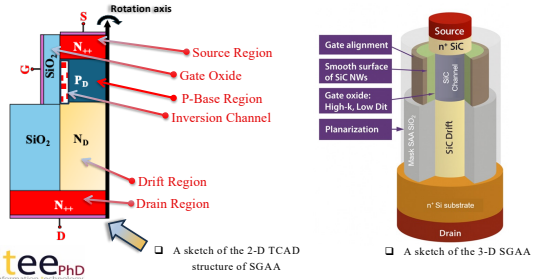
[2] SiC Gate All around MOSFETs

Objective:

Analysis and identification of design techniques for power SiC MOSFETs with **gate-all-around (SGAA)** architecture.

Methodology:

Study and validation of device design through **TCAD** simulations.



❑ A sketch of the 2-D TCAD structure of SGAA

❑ A sketch of the 3-D SGAA

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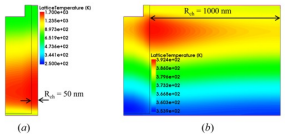
[2] Key Properties of SiC Gate-All-Around MOSFETs

- ✓ **Cylindrical Symmetry** – Provides uniform electric field distribution, reducing hot spots. ☑
- ✓ **Lower Specific On-Resistance** R_{DSon} improved current conduction efficiency for the same chip area. ☑
- ✓ **Higher Breakdown Voltage Capability** – Optimized electric field profile allows higher blocking voltages. ☑
- ✓ **Reduced Gate Charge** – Enables faster switching speeds and lower switching losses. ☑
- ✓ **Low Thermal Conductivity** of the surrounding oxide. ☒



*Low thermal conductivity of the surrounding oxide, combined **with high current density**, causes severe localized heating during short-circuit events.*

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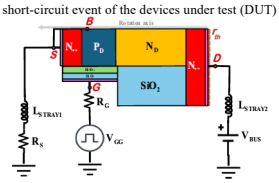
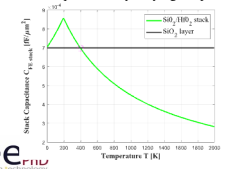
[2] Ferroelectric material integration HfO_2

- Electro-thermal mixed-mode circuit used to simulate the short-circuit event of the devices under test (DUT)

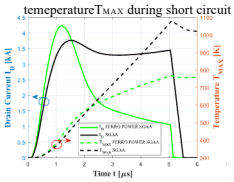


- **Electro-thermal mixed-mode** circuit parameters
  - R_S, L_{STRAY1}, L_{STRAY2} : *those serve to emulate the parasitic effets of the packaging.*
  - R_G : *internal resistance of generator*
  - V_{GG} : *gate-connected pulse source*
  - V_{BUS} : *supply voltage*
  - r_{th} : *surface thermal resistance* $\left[\frac{K \cdot cm^2}{W}\right]$

- Gate capacitance by varying temperature T



- Drain current I_D and Max temeperatureT_{MAX} during short circuit



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Publications during the PhD

1. C. Terraciano, A. Borghese, M. Boccarossa, V. d'Alessandro, and A. Irace, "A geometry–scalable physically–based SPICE compact model for SiC MPS diodes including the snapback mechanism," Solid State Phenomena, 2024.

2. A. Borghese, V. Terraciano, M. Boccarossa, A. Irace, and V. d'Alessandro, "A geometry–scalable electrothermal compact circuit model of SiC merged–PiN–Schottky diodes accounting for the snapback mechanism: Application to current surge events," Microelectronics Reliability, 2025.

3. L. Maresca, V. Terraciano, A. Borghese, M. Boccarossa, M. Riccio, G. Breglio, A. Mihaila, G. Romano, S. Wirths, L. Knoll, and A. Irace, "SiC GAA MOSFET Concept for High Power Electronics Performance Evaluation Through Advanced TCAD Simulations," Solid State Phenomena, 2024.

4. L. Maresca, V. Terraciano, A. Borghese, M. Boccarossa, M. Riccio, G. Breglio, S. Wirths, and A. Irace, "Evaluation of switching performances and short-circuit capability of a 1.2 kV SiC GAA MOSFET through TCAD simulations," Key Engineering Materials, 2025.

5. V. d'Alessandro, V. Terraciano, A. Borghese, M. Boccarossa, and A. Irace, "A simple electrothermal compact model for SiC MPS diodes including the snapback mechanism," International Workshop on Thermal Investigations of ICs and Systems (THERMINIC), Budapest, Hungary, 2023.

6. C. Scognamillo, A. Borghese, K. Melnyk, I. Nistor, V. d'Alessandro, M. Boccarossa, V. Terraciano, M. Riccio, A. P. Catalano, G. Breglio, N. Lophitis, M. Antoniou, M. Rahimo, A. Irace, and L. Maresca, "Out-of-SOA Performance of 3.3 kV SiC MOSFETs: Comparison Between Planar and Quasi-Planar Trench," SIE Conference, Cham, 2025.

7. V. Terraciano, A. Borghese, C. Ceresa, V. d'Alessandro, and A. Irace, "Optimal bonding of 4H–SiC parallel diodes in a single TO-247 package for improved surge current robustness: experimental investigation," ESREF Conference, Bordeaux, France, 2025.

8. A. Borghese, M. Boccarossa, V. Terraciano, L. Maresca, M. Riccio, and A. Irace, "Effect of the Load Inductor on the Avalanche Ruggedness of 1200-Volt Silicon Diodes during Unclamped Inductive Switching, ESREF Conference, Bordeaux, France, 2025..

9. V. Terraciano, A. Borghese, M. Boccarossa, A. Irace, G. A. Salvatore, and L. Maresca, "Electrothermal performance enhancement of silicon carbide gate-all-around MOSFETs using a ferroelectric gate stack," THERMINIC Conference, Naples, Italy, 2025.

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Thank You For Your Attention

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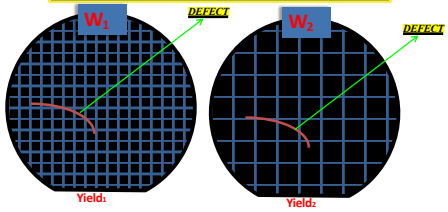
[1] Boosting Yield: Multi-Die Integration in Power Diodes

$$Yield = \frac{good\ dice}{N} \qquad N = total\ die\ count\ on\ a\ wafer$$

$Yield_1 > Yield_2$



Device manufacturers commonly embed **two SiC dies in parallel within the same package** to *increase current capability*. This approach offers two key advantages: (i) **it improves the fabrication process yield**, and (ii) **it avoids modifications to the existing semiconductor production line**.

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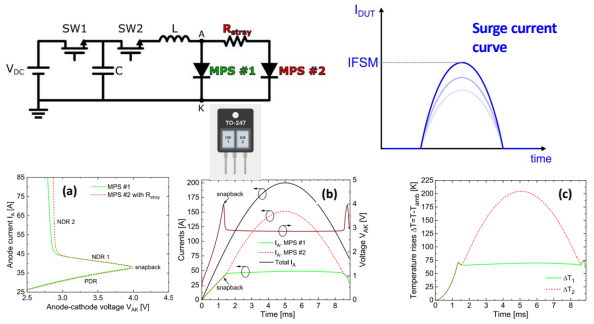
[1] Merged PiN Schottky: Circuit Model Application



(a) I-V Forward Curve by varying of two MPS, (b) currents of two MPS during dynamic SPICE simulation of the surge test (c) Temperature by varying time

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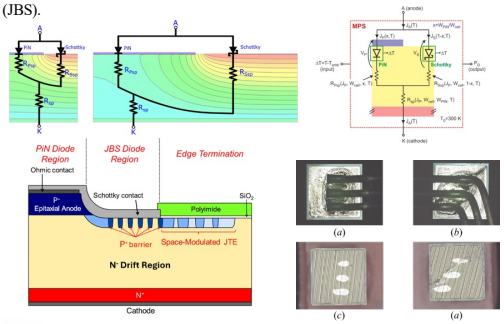
Research activities

1. Circuit-level modeling and experimental characterization of Silicon Carbide (SiC) power diodes: **Merged PiN Schottky** (MPS) and **Junction Barrier Schottky** (JBS).



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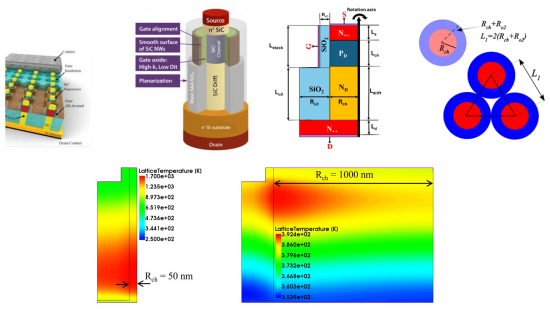
Research activities

2. Design, analysis, and development of an innovative Silicon carbide **Gate-All-Around** (SGAA) power MOSFET architecture.



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4H-Silicon Carbide

Silicon carbide (SiC) belongs to the class of wide-bandgap materials, i.e., semiconductors showcasing a forbidden energy band wider than silicon (Si).

Advantages of SiC respect than Si for *power electronic devices*:

- *Higher thermal conductivity*
- *Higher working temperature*
- *Higher saturation velocity*
- *Higher breakdown voltage*

Properties	Silicon	4H-SiC
Energy Bandgap (eV)	1.1	3.2
Relative Dielectic Constant	11.7	9.7
Thermal Conductivity (W/cmK)	1.5	3.7
Electron Affinity (eV)	4.05	3.7
Density of States Conduction Band (cm^{-3})	2.80×10^{19}	1.23×10^{19}
Density of States Valance Band (cm^{-3})	1.04×10^{19}	4.58×10^{18}

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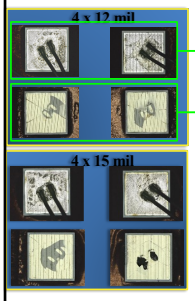
Failure mechanism of standard bond-wire configuration



Left and right die after chemical decapsulation

After delayering process

Chemical Decapsulation (SiC Diodes)

- **Step 1 – Mold Compound Removal**
  - Acid Bath with H_2SO_4, 180 °C, 5 min
- **Step 2 – Aluminum Delayering**
  - Aqua Regia ($HCl + HNO_3$)
- **Precautions**
  - Fume hood + PPE (gloves, goggles)
  - Rinse with DI water between steps
  - Careful time control → avoid layer damage

In the 4×12 mil and 4×15 mil configurations, both dies within the package exhibited **Failure Type 2** characteristics, including severe metal melting and structural damage. For both configurations, and at both tested temperatures (25 °C and 110 °C), the observed failure mode consistently corresponded to Type 2.

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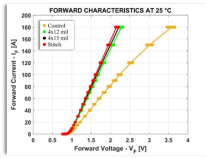

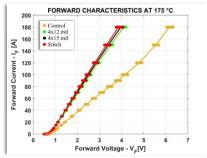

Name Surname

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