UNIVERSITÀ DEGLI STUDI DI NAPOLI FEDERICO II

DOTTORATO DI RICERCA / PHD PROGRAM IN
INFORMATION TECHNOLOGY AND ELECTRICAL ENGINEERING

Activities and Publications Report

PhD Student: Vincenzo Terracciano

Student DR number: DR996633

PhD Cycle: XXXVIII
PhD Chairman: Prof. Stefano Russo

PhD program student's start date: 01/11/2022
PhD program student's end date: 31/10/2025

Supervisor: Andrea Irace

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PhD scholarship funding entity:
University of Naples Federico II

General information

Vincenzo Terracciano received in 2022 the Master of Science degree in Electronic Engineering from the University of Naples Federico II.
Within the PhD program in Information Technologies and Electrical Engineering (ITEE), he attended the curriculum in Electronics Engineering.
He received an industrial PhD grant funded jointly by the University of Naples Federico II and Vishay Semiconductor Italiana S.p.A. (Borgaro Torinese, Italy), as part of the national program for industrial PhDs.

Study activities

Attended Courses

Year	Course Title	Type	Credits	Lecturer	Organizer(s)
1rd	Academic Entreprenuership	Ad Hoc course	4	Prof. Pierluigi Rippa	ITEE
1rd	How to boost yourPhD	Ad Hoc course	4	Dr. Antigone Marino	ITEE
1rd	Electrodynamics of Continuous Media	course	9	Prof. Claudio Serpico	ITEE
2rd	Numerical Methods For Thermal Analysis, Modeling, And simulation: Application to Electronic Devices And systems.	Ad Hoc course	4	Dr. Antonio Pio Catalano	ITEE
2rd	Modelli Numerici per i Campi	course	9	Prof. Massimiliano d'Acquino	ITEE
3rd	Fiber Optic Sensing And Optoelectronic Circuits: Design And Application	Ad Hoc Course	4	Dr.Vincenzo Romano Marrazzo	ITEE

Attended PhD Schools

PhD Year	School title	Location	Credits	Dates	Organization
1rd	CI-LAM 2023	Napoli, Italy	4	17-21/07/2023	University of Naples

Attended Seminars

PhD Year	Seminar Title	Credits	Lecturer	Lecturer affiliation	Organization
1rd	Quantum Complexity	0.2	Prof. Alioscia Hamma		SSM
1rd	SSM Scientific Colloquia	0.2	Prof. Pietro DeLellis		SSM
1rd	2023-Industry 4.0 Fundamentals in Bosch Applications	2	Eng. MartinoBruni	BOSCH	
1rd	The Hours of the Sun. Astronomy, Geometry, and Art in Ancient Sundials	0.2	Prof. Alessandra Pagliano		SSM
1rd	Teoresi gruop	0.4	Prof. Giuseppe Ruello	Teoresi Group	
1rd	Cylindrical Micro- and Nanowires: From Curvature Effects on Magnetization to Sensing Applications	0.2	Prof. Manuel Vázquez		ITEE
1rd	Modeling Clustered Seismicity Risk: AreWe Ready?	0.2	Prof. paolo Bazzurro		ITEE
1rd	Traffic Engineering with Segmented Routing: optimally addressing popular usecases	0.2	Prof. Pascal Merindol		ITEE
1rd	Fulbrighters Fredericiani aIngegneria	0.4	Prof. Giuseppe Ruello Prof. Riccardo Lattanzi		ITEE
1rd	Insights int the Design of Transmit and Receive Coils for Ultra-High Field MRI	0.4	Prof. Riccardo Lattanzi		ITEE
1rd	BGP & Hot-Potato Routing: graceful and optimal convergence in case of IGP events	0.2	Prof. Pascal Merindol		ITEE
1rd	Optimization of a mobile clinic routingand scheduling problem in equitable vaccination outreach	0.2	Prof.MingyaoQi		ITEE
1rd	Introduction to Formal Verification of Digital Design and Jasper Apps	0.4	Ing.Massimo Roselli (Company: Cadence)		ITEE

2rd	Reliability Against CERN's Radiation Environment	0.2	Dr. .Salvatore Denzeca-CERN, Geneva		ITEE
2rd	Silicon Carbide - New Challenges	0.4	Dr. Danilo Crippa (sede Vishay-Semiconductor)	Vishay semiconductor	
2rd	Intelligenza Artificiale E Regole Del Mercato	0.4	Massimo Rubino de Ritis		ITEE
2rd	Verso Una Gestione Smart Della Risorsa Idrica Con Il Supporto Della Digital Innovation	0.4	Enrica Menduni de Rossi		ITEE
2rd	FEOL and BEOL: fanding boundries	0.4	Prof. Luciano Sacltrito	Vishay semiconductor	
2rd	Machine Deception	0.2	Dr. Henrik Skaug Sætra		ITEE
2rd	Sustainable: Strategies And Best Practices For A Green Engineering Future	1	Annalisa Di Leva, Dimitri Cuomo, Benedetta Ramazzotti, Tiziano Marcozzi		ITEE
2rd	Modeling Clustered Seismicity Risk: AreWe Ready?	1	Annalisa Di Leva, Cynthia Cuvi, Giulia Favale, Alessio Zoccoli		ITEE
2rd	Social Network Analysis: Methods and Applications	0.4	Prof. Tanmoy Chakraborty		ITEE
2rd	Introduction to Large Language Models: Evolution and the current state	0.4	Prof. Tanmoy Chakraborty		ITEE
2rd	Towards the Sustainable Vehicle Era	0.4	Massimo carbone-Sr.Director E-mobility Applications	Vishay Semiconductor	ITEE
2rd	From ACE Technologies to Sustainable, Accessible and Equitable Urban Mobility: An Optimization Journey	0.4	Prof. Mauro Salazar		ITEE

Research activities

The research conducted in the final PhD year focused on the electrothermal modeling and reliability assessment of silicon carbide (SiC) power devices for high-efficiency and high-reliability power electronics. The study developed a geometry-scalable, physically based SPICE modeling framework for Junction Barrier Schottky (JBS) and Merged PiN Schottky (MPS) diodes, capable of accurately reproducing conduction, thermal, and snapback phenomena. The models were validated through TCAD simulations and extensive experimental characterization under static and dynamic conditions. In parallel, the work investigated an innovative 1.2 kV SiC Gate-All-Around (GAA) MOSFET concept by means of mixed-mode electrothermal TCAD simulations, analyzing its superior electrostatic performance and thermal limitations under short-circuit stress. To mitigate these effects, a ferroelectric (HfO_2)-based gate stack was proposed, achieving current self-limiting behavior and enhanced short-circuit robustness. Overall, the research provided new design and modeling methodologies to optimize the performance and reliability of next-generation SiC power devices

Credits summary

PhD Year	Courses	Seminars	Research	Tutoring / Supplementary Teaching
1st	21	5.2	37.2	0
2nd	13	5.6	45.4	0
3rd	4	0	48.6	0

Research periods in institutions abroad and/or in companies

PhD Year	Institution / Company	Hosting tutor	Period	Activities
2-3st	Vishay Semiconductor	Nabil El baradi	15/02/2024 23/10/2025	During this period, I focused on the modeling, electrothermal characterization, and reliability analysis of SiC power devices developed within Vishay's R&D department. My work included experimental testing, surge-current robustness analysis, and the development and validation of advanced SPICE and TCAD modeling frameworks for industrial applications.

PhD Thesis

The progressive electrification of society—from sustainable mobility to energy conversion and distribution—is accelerating the demand for power electronic devices with high efficiency, reliability, and power density. In this context, silicon carbide (SiC) has emerged as an enabling material thanks to its wide bandgap, high critical electric field, and reduced conduction and switching losses, making it particularly attractive for automotive and, more broadly, electrified transportation. This dissertation is organized into two complementary research thrusts, focused on the modeling, development, and experimental characterization of SiC power devices. The

first thrust develops a scalable electrothermal circuit-level modeling framework for Junction Barrier Schottky (JBS) and Merged PiN Schottky (MPS) diodes, accompanied by experimental characterization under static and dynamic conditions. The proposed SPICE models are physically grounded and capture conduction and loss mechanisms, including temperature effects, self-heating, and—specifically for MPS—the snapback phenomenon. Model validation is carried out against TCAD data, demonstrating accuracy, numerical robustness, and portability to SPICE-like simulators. In addition, for a specific class of 1.2 kV JBS diodes, an experimental campaign with failure analysis is conducted to optimize wire bonding strategies at die level, with the goal of improving surge-current robustness. The second thrust introduces and analyzes an innovative 1.2 kV SiC Gate-All-Around (GAA) MOSFET concept, investigated through static, dynamic, and mixed-mode electrothermal TCAD simulations. The channel—fully wrapped at 360◦ by the gate oxide—enables superior electrostatic control; furthermore, the absence of a termination region (and the resulting increase in active area) improves the trade-off between specific on-resistance and blocking capability. However, being fully surrounded by silicon dioxide, the SiC GAA MOSFET exhibits limited capability to handle thermal stress, particularly during short-circuit events. To address this, the final part of the dissertation proposes a solution based on a ferroelectric (HfO_2) gate stack to restrain current and thus self-heating during short-circuit transients. Finally, the work discusses design criteria, static/dynamic performance metrics, and technology-integration implications.

Research products

List of scientific publications

International journal paper

A. Borghese, V. Terracciano, M. Boccarossa, A. Irace, and V. d'Alessandro,
A geometry–scalable electrothermal compact circuit model of SiC merged–PiN–Schottky diodes accounting for the snapback mechanism: Application to current surge events,
Microelectronics Reliability,
168:115668, 2025. DOI: 10.1016/j.microrel.2025.115668.

International journal paper

V. Terracciano, A. Borghese, M. Boccarossa, V. d'Alessandro, and A. Irace,
A geometry–scalable physically–based SPICE compact model for SiC MPS diodes including the snapback,
mechanism,
Solid State Phenomena,
360:67–74, 2024. DOI: 10.4028/p-b9ImzL.

International journal paper

L. Maresca, V. Terracciano, A. Borghese, M. Boccarossa, M. Riccio, G. Breglio, A. Mihaila, G. Romano, S. Wirths, L. Knoll, and A. Irace.
SiC GAA MOSFET Concept for High Power Electronics Performance Evaluation Through Advanced TCAD Simulations,
Solid State Phenomena,
360:75–80, 2024. DOI: 10.4028/p-lhRi4M.

International journal paper

L. Maresca, V. Terracciano, A. Borghese, M. Boccarossa, M. Riccio, G. Breglio, S. Wirths, and A. Irace,
Evaluation of switching performances and short-circuit capability of a 1.2 kV SiC GAA MOSFET through TCAD simulations,
Key Engineering Materials
1021:17–23, Sep. 2025. DOI: 10.4028/p-Mc0tPH.

International conference paper

V. d'Alessandro, V. Terracciano, A. Borghese, M. Boccarossa, and A. Irace,
A simple electrothermal compact model for SiC MPS diodes including the snapback mechanism,
International Workshop on Thermal Investigations of ICs and Systems
Budapest, Hungary, Sep. 2023. DOI: 10.1109/THERMINIC60375.2023.10325871.

International conference paper

V. Terracciano, A. Borghese, M. Boccarossa, A. Irace, G. A. Salvatore, and L. Maresca,
Electrothermal performance enhancement of silicon carbide gate-all-around MOSFETs using a ferroelectric gate stack,
in Proc. International Workshop on Thermal Investigations of ICs and Systems (THERMINIC 2025)
Naples, Italy, Sep. 2025. To appear (IEEE Xplore).

International conference paper

V. Terracciano, A. Borghese, C. Ceresa, V. d'Alessandro, A. Irace,
Optimal bonding of 4H–SiC parallel diodes in a single TO-247 package for improved surge current robustness: experimental investigation,
in Proc. European Symposium on Reliability of Electron Devices, Failure Physics and Analysis (ESREF 2025)
Bordeaux, France, Oct. 2025. Preprint available on HAL; extended journal version in Microelectronics Reliability (forthcoming).

International conference paper

Borghese, M. Boccarossa, V. Terracciano, L. Maresca, M. Riccio, A. Irace,
Effect of the Load Inductor on the Avalanche Ruggedness of 1200-Volt Silicon Diodes during Unclamped Inductive Switching,
in Proc. European Symposium on Reliability of Electron Devices, Failure Physics and Analysis (ESREF 2025)
Bordeaux, France, Oct. 2025. Preprint available on HAL; extended journal version in Microelectronics Reliability (forthcoming).

National conference papers

C. Scognamillo, A. Borghese, K. Melnyk, I. Nistor, V. d'Alessandro, M. Boccarossa, V. Terracciano, M. Riccio, A. P. Catalano, G. Breglio, N. Lophitis, M. Antoniou, M. Rahimo, A. Irace, and L. Maresca,
Out-of-SOA Performance of 3.3 kV SiC MOSFETs: Comparison Between Planar and Quasi-Planar Trench,
Proceedings of SIE 2024, Lecture Notes in Electrical Engineering, vol. 1263,
Genoa, Italy, 2024, pp. 369–374, Publisher: Springer, DOI: 10.1007/978-3-031-71518-1_44,

Awards and Prizes

Best Paper Award – International Workshop on Thermal Investigations of ICs and Systems (THERMINIC 2025), Naples (Italy), 24–26 Sep 2025.
Paper: Electrothermal performance enhancement of silicon carbide gate-all-around MOSFETs using a ferroelectric gate stack.
Authors: V. Terracciano, A. Borghese, M. Boccarossa, A. Irace, G. A. Salvatore, L. Maresca.

Date 21/10/2025

PhD student signature

Supervisor signature