Giovanni Maria Capuano

Onboard AI for Near Real-Time Delivery of Critical Insights from Spacecraft

Tutor: Prof. Strollo

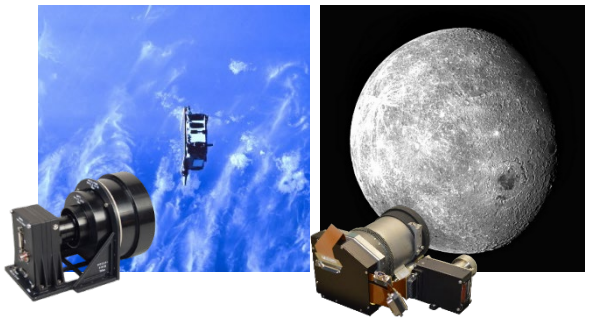
co-Tutor: Prof. Petra

Cycle: XXXVIII

Year: 2

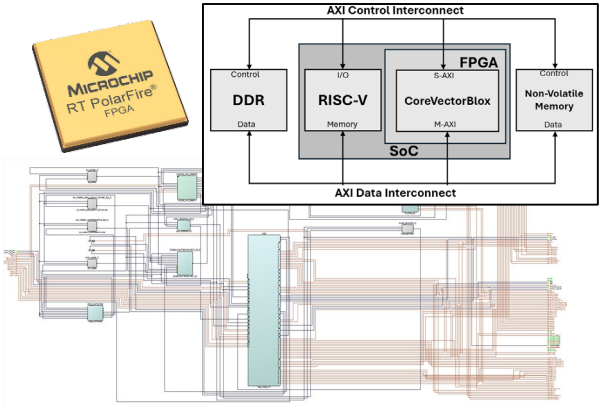
Candidate's information

- MSc degree in **Electronic Engineering @DIETI – Federico II**
- DIETI Research group/laboratory: **VLSI Group**
- PhD start date: **01/11/2022** – end date: **31/10/2025**
- Scholarship type: **PNRR – DM 352**
- Partner company: **Techno System Development (TSD-Space)**
- Periods in company: 12 Months (completed)
- Abroad Research Institution: **The European Space Research and Technology Centre (ESTEC) of ESA (Noordwijk, Netherlands)**
- Period abroad: 03/02/2025 – 03/08/2025



Summary of study activities

- AI-based Object Detection (OD) on optical satellite imagery
- AI-based Super-Resolution (SR) on optical satellite imagery
- FPGA-based HW acceleration of Deep Learning algorithms



Ad hoc PhD Course

- ✓ Numerical Methods For Thermal Analysis, Modeling, and Simulation: Application to Electronic Devices and Systems (Prof. Antonio Pio Catalano)
- ✓ Industrial Embedded Systems Design with the ARM Architecture (Prof. Barbareschi)
- ✓ Machine Learning for Science and Engineering Research (Prof. Anna Corazza)

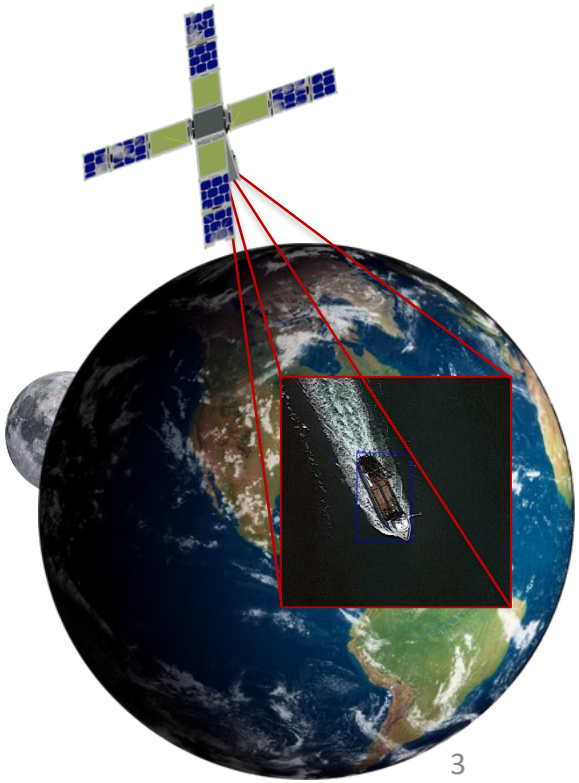
Conference

- ✓ International Astronautical Congress (IAC24), Milan (Oral presentation)
- ✓ SPAICE: AI in and for space, (ECSAT by ESA), Didcot (UK) (Oral Presentation)
- ✓ SciTech, American Institute of Aeronautics and Astronautics, Orlando (USA) (next 6-10 January 2025) (Oral Presentation)

Workshop

- ✓ Italian Space Agency Workshop, L'impegno Italiano nel Settore dei CubeSat: Tecnologie e Missioni Future (Oral presentation)
- ✓ Italian Space Agency Workshop, Tecnologie Spaziali di ASI (Oral Presentation)

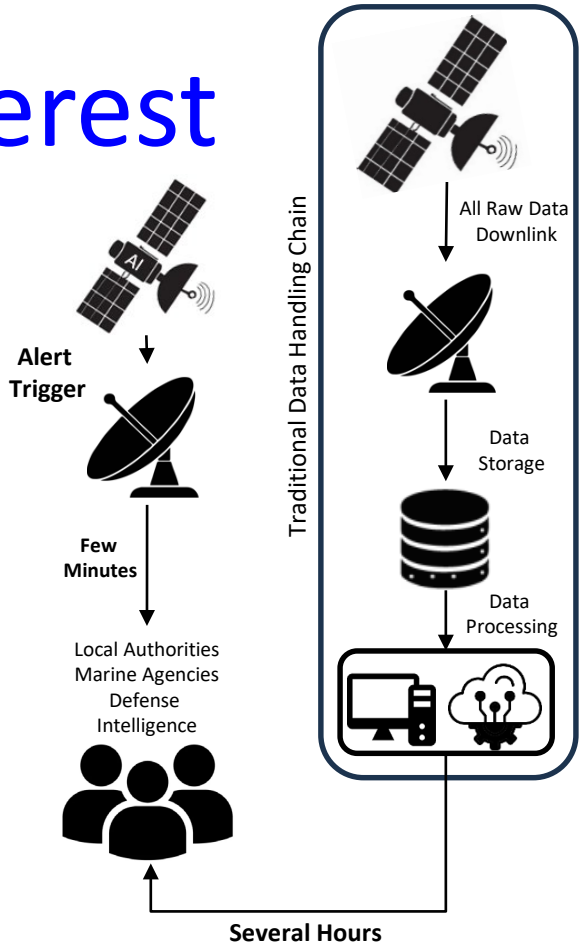
Seminar



Research field of interest

Rapid Alerts in Earth Observation - Accurate target & hazard detection and **timely information extraction** play a key role in a wide range of surveillance and monitoring operations:

- Emergency Response
- Illegal activity monitoring
- Military Reconnaissance



Problem: Accurate & Reliable Target Detection

Small Size of Objects | Limited Spatial Resolution | Complex Background → Frequent Misdetection

Problem: Rapid Alerts & Critical insights Delivery

Limited Downlink Bandwidth | Ground Station Availability | Fast Amount of Data Collected → **Delay**

Solution

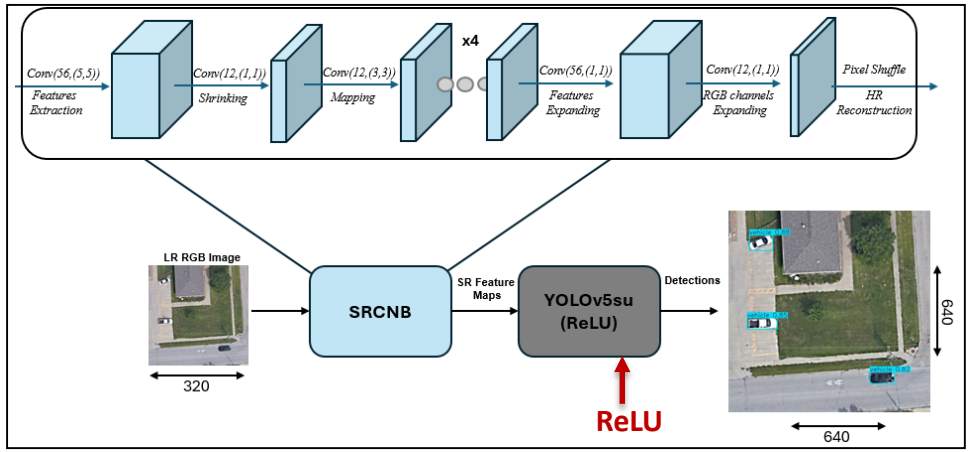
Edge Computing
FPGA-based HW Acceleration

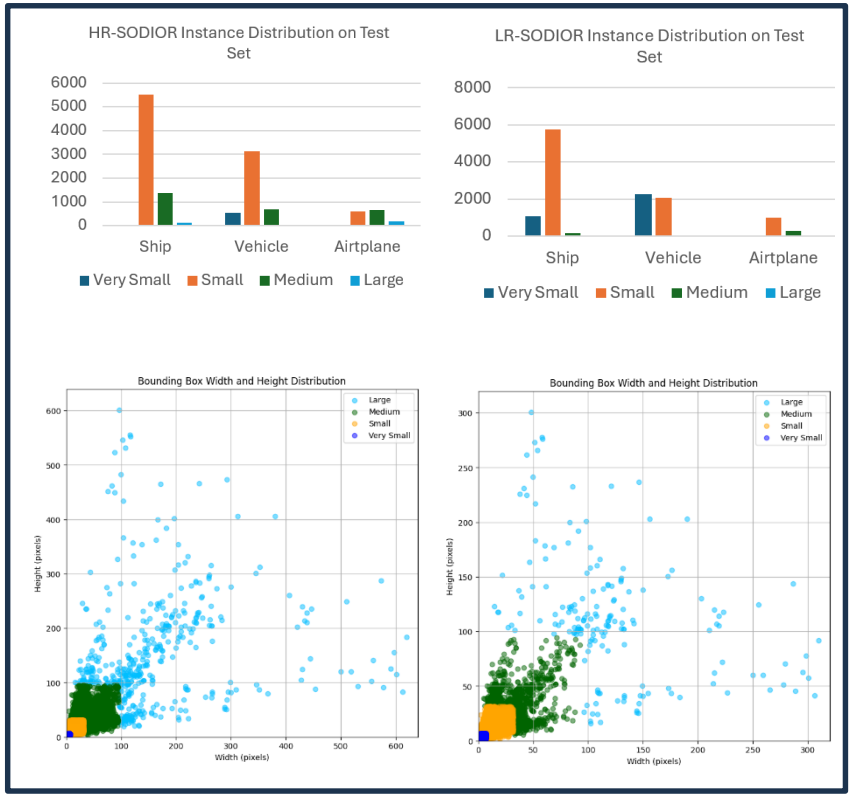
SR for Object Detection
(AI-based)

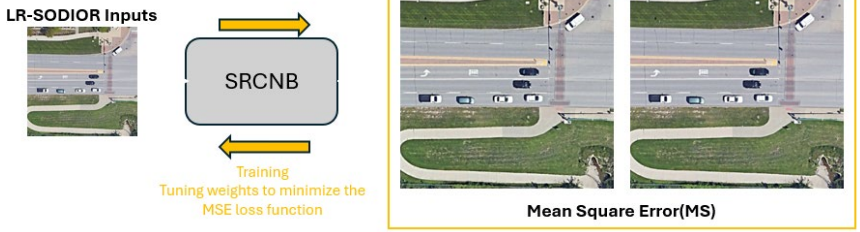
itee PhD
information technology
electrical engineering

Super-Resolution for Object Detection Results

SR-YOLOv5 is an enhanced version of the YOLOv5 object detector that integrates an SR backbone (**SRCNB**) for the improvement of small object detection performances







An inference overhead of 0.6 ms on the A100 GPU

Table 1 Super Resolution Results

Model	PSNR [dB]	SSIM	N° Param.
SRCNN	33.74	0.92	20,099
FSRCNN	34.03	0.93	24,683
ESPCN	34.40	0.93	26,647
EDRN	36.28	0.94	1,395,788
SRCNB	34.47	0.93	16,960

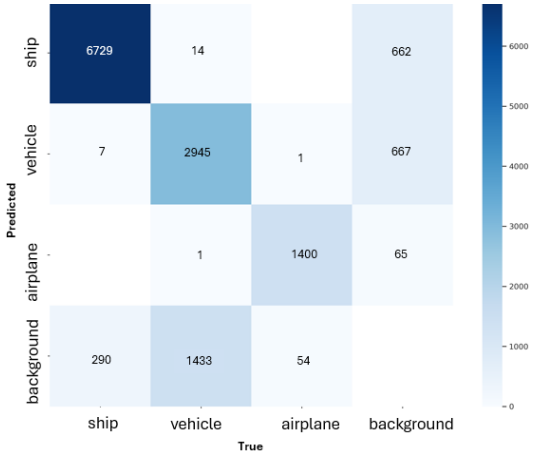
Table 2 Object Detection Results

Model	Input Size	Param.	mAP50	mAP50:95
YOLOv5su (ReLU)	640	9,123,337	0.836	0.590
YOLOv5su (SiLU)	640	9,123,337	0.935	0.792
YOLOv5su (SiLU)	320	9,123,337	0.920	0.761
SR-YOLOv5su (ReLU)	320	9,140,297	0.912	0.756

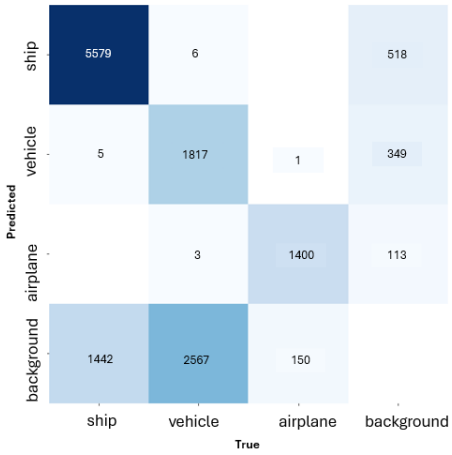
Super-Resolution for Object Detection Results

By incorporating the SRCNB, the OD network improves its ability to detect small objects and differentiate them from the background, leading to a reduction in FN and FP compared to using the OD with native-resolution images

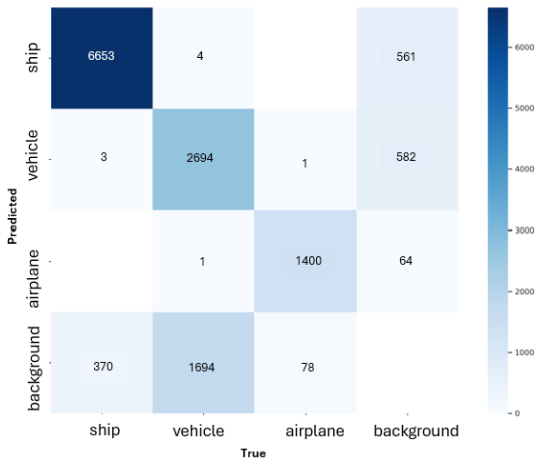
YOLOv5su Confusion Matrix HR-SODIOR



YOLOv5su Confusion Matrix LR-SODIOR



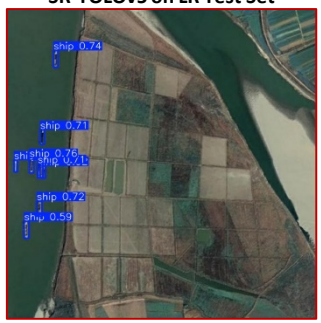
SR-YOLOv5su Confusion Matrix LR-SODIOR



SR-YOLOv5 on LR Test Set

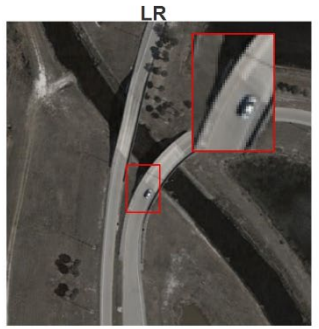
YOLOv5 on LR Test Set

SR-YOLOv5 on LR Test Set



YOLOv5 on LR Test Set

SR Results



FPGA-based HW Acceleration Results

- **PolarFire SoC FPGA:** A power-efficient edge computing platform for deploying AI onboard spacecraft

Five Core Linux Capable Hard RISC-V	Non-Volatile Flash-based FPGA	Low Power Consumption w.r.t SRAM FPGA	Radiation-induced Upset tolerant w.r.t SRAM FPGA

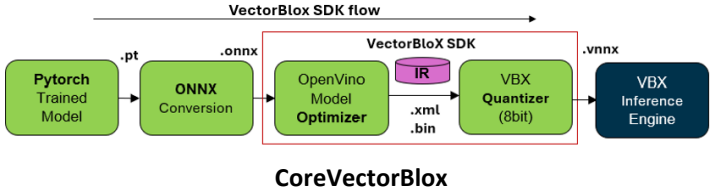
PolarFire RT SoC for challenging long-time duration or deep space missions

- CoreVectorBlox, an FPGA-based hardware accelerator for CNNs

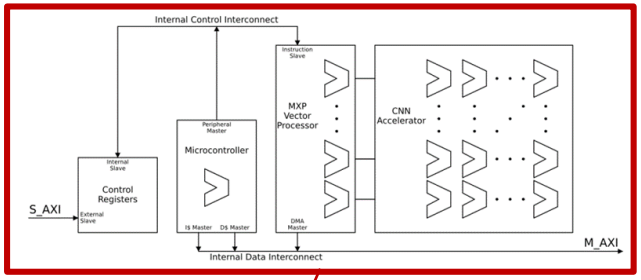
Overlay HW Architecture	**Specialized to execute network BLOB instructions**	**Well-suited for power-sensitive edge computing scenario**

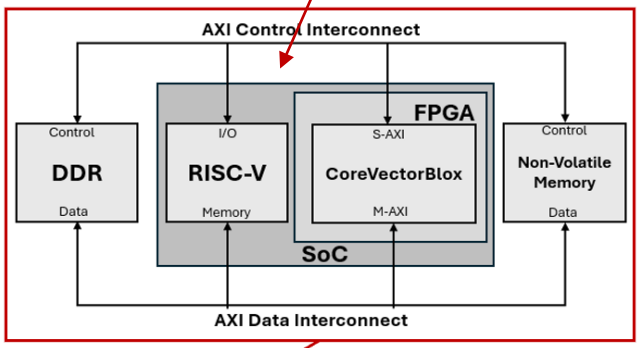
Table 3 AI Engine Performance Results

Device	Precision	mAP50	Inference Speed	Avg. Power	Avg. Energy
A100	FP32	0.9120	7.3 ms	~ 53.04 W	~ 387,2 mJ/frame
Jetson Orin Nano	FP32	0.9120	20 ms	~ 9.6 W	~ 192 mJ/frame
Jetson Orin Nano	INT8	0,8298	16 ms	~ 8,85 W	~ 141,6 mJ/frame
PolarFire SoC	INT-8	0.9110	55 ms	~ 2.46 W	~ 135,3 mJ/frame



CoreVectorBlox





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Resource Usage
+----------------+--------+--------+------------+
| Type           | Used   | Total  | Percentage |
+----------------+--------+--------+------------+
| 4LUT           | 148083 | 254196 | 58.26      |
| DFF            | 146893 | 254196 | 57.79      |
| I/O Register   | 0      | 370    | 0.00       |
| Logic Element  | 184157 | 254196 | 72.45      |
+----------------+--------+--------+------------+
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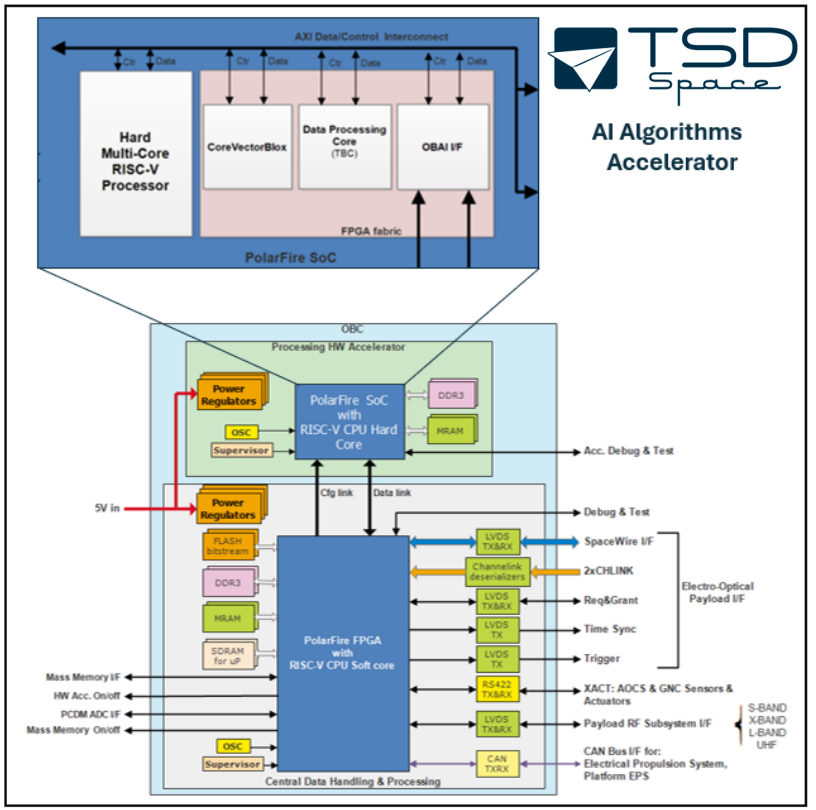
Company Activities Overview

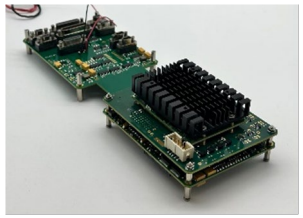
EarthNext Mission: EarthNext is a 16U CubeSat mission developed as part of the Italian Space Agency's Alcor Program, aiming to demonstrate multispectral imaging of the Earth from a very-low Earth orbit. **Main Activity**: Deployment of AI-based algorithms onboard TSD-Space's OBC.

FOPAC Project: FOPAC's goal is to develop an active motion control system for the focal plane of electro-optical payloads used in Earth observation applications to enhance image quality in terms of spatial resolution and signal-to-noise ratio. **Main Activity**: Development of multiple image super-resolution algorithms.

ANHEO Project: An integrated unit for autonomous absolute and relative navigation of nano- and microsatellites. **Main Activity**: FPGA hardware design and deployment of AI-powered, vision-based navigation algorithms.

IRIDE VHR Mission: The VHR satellite within the IRIDE constellation is equipped with a high-performance optical imager, currently under development by TSD-Space (FPA and CE) in collaboration with Media Lario (Optics). **Main Activity**: Designing in-orbit calibration and maintenance procedures for the electro-optical payload.





Research Activities: Feature Development

- Performance Evaluation of Object Detection on Optical Satellite RAW Data
- VHDL development for data pre-processing, including inline calibration, and geometric/atmospheric correction, to enhance onboard detection capabilities.
- Benchmarking across different hardware platforms: FPGAs, embedded GPUs, and ASICs (e.g., VPU & TPU).
- Exploration of triple modular redundancy (TMR) FPGA configurations for AI acceleration to enhance reliability in the space environment.
- Exploration of commercial off-the-shelf (COTS) multi-gigabit standard interfaces for transferring RAW data from electro-optical payloads to COTS processing units, in time-sensitive Earth observation applications (Research Activity in ESTEC)

Research products

[P1]	Giovanni Maria Capuano, Salvatore Capuozzo, Antonio G.-M. Strollo, Nicola Petra *Super-Resolution-Based Small Object Detection for Real-Time Surveillance and Monitoring: An Onboard Satellite FPGA Implementation,* **75th International Astronautical Congress (IAC), Milan, Italy** (Scopus Indexed)
[P2]	Giovanni Maria Capuano, Salvatore Capuozzo, Antonio G.-M. Strollo, Nicola Petra *FPGA-Based Hardware Acceleration for Real-Time Maritime Surveillance and Monitoring Onboard Spacecraft,* **SPAICE 2024: The first joint Eurpoean Space Agency /IAA Conference on AI in and for Space** (NASA ADS Indexed)
[P3]	G.M. Capuano, G. Napolano, V. Capuano, A. G.M. Strollo, N. Petra, G. Cuciniello, E. Zaccagnino, G. Varacalli *FPGA Hardware Acceleration for Deep Learning-based Satellite Pose Estimation,* **American Institute of Aeronautics and Astronautics (AIAA) SciTech Conference** (Accepted)
[P4]	G. Leccese, S. Natalucci, L. Iannascoli, M. Melozzi, A. Turella, E. Piersanti, M. Duzzi, F. Trezzolani, G. M. Capuano, T. A. La Marca, M. D. Graziano, M. Grassi, V. Fortunato, P. De Marchi, C. Cardenio. *Preliminary Design and Perspectives of the EartNext Cubesat Mission for Earth Observation from Very Low Earth Orbit* **Small Satellite Systems and Services Symposium (4S Symposium) 2024**


ship 0.95
airplane 0.89
airplane 0.91
vehicle 0.88
vehicle 0.88
vehicle 0.78
airplane 0.90
airplane 0.88
airplane 0.91

THANK YOU