Alberto Moriconi

An Automatic Methodology for the Synthesis of Approximate Circuits

Tutor: Prof. Nicola Mazzocca

Cycle: XXXVII Year: Third

Candidate's information

- Holds a MSc degree in Computer Engineering
- Worked with the SECLAB / Embedded Systems Laboratory
- PhD started on 1/11/2021, ends on 30/11/2024
- No scholarship
- Experience as embedded systems engineer in Rete Ferroviaria Italiana S.p.A.

Summary of study activities

- Study activities has been roughly divided between three topics:
  - Study of the relevant literature on the topics of Approximate Computing
  - Study in fields where the Approximate Computing paradigm is appliable (particular focus on ML and image processing topics)
  - Study related to software engineering flows and certification flows for safety critical systems, due to the parallel research effort in those fields

Research area(s)

- Amount of data to be processed is increasing, power consumption concerns are becoming increasingly critical
- Approximate computing is a possible approach: we “gently” relax, in a controlled way, correctness requirements of specific applications (especially iterative or strictly tied to human perceptual limitations)
- In this way, we can obtain area, time or power consumption advantages

Research results

- The problem of approximation of combinatorial circuits is approached by a fully automatic methodology and tool based on non-trivial local rewriting of and-inverter graphs, obtained by describing the optimization problem as a Satisfiability Modulo Theories (SMT) problem and applying multi-objective optimization to gradually introduce the approximation, providing state-of-the-art improvements in the resulting circuit area.
- While directly tailored for ASICs, the proposed methodology is then shown to be able to successfully address approximation of circuits targeting FPGAs, obtaining notable improvements in the resulting circuit switching activity.
- A number of improvements for the FPGA case is then applied, by devising a switching activity-based energy dissipation model to use as an optimization metric and by exploiting specific approaches based on properties of the underlying circuits (specifically the use of Grobner bases for error evaluation of arithmetic circuits) in order to reduce the complexity of the optimization problem and allow the methodology to be applied to bigger circuits.

Research products

Approximate computing

International journal papers

M. Barbareschi, S. Barone, N. Mazzocca, A. Moriconi,
A catalog-based AIG-rewriting approach to the design of approximate components,
IEEE Transactions on Emerging Topics in Computing,
11(1), 70-81, 2022, DOI: 10.1109/TETC.2022.3170502

M. Barbareschi, S. Barone, N. Mazzocca, A. Moriconi,
FPGA approximate logic synthesis through catalog-based AIG-rewriting technique,
Journal of Systems Architecture,
150, 103112, 2022, DOI: https://doi.org/10.1016/j.sysarc.2024.103112

Book chapters

M. Barbareschi, S. Barone, N. Mazzocca, A. Moriconi,
Design Space Exploration Tools
In: A. Bosio, D.Ménard, O. Sentieys (eds) Approximate Computing Techniques: From Component- to Application-Level,
215-259, Springer, Cham, 2022, DOI: https://doi.org/10.1007/978-3-030-94705-7_8

Safety critical applications in the railway domain

International journal papers

A. Amendola, M. Barbareschi, S. De Simone, G. Mezzina, A. Moriconi, C. L. Saragaglia, D. Serra, D. De Venuto,
A real-time vital control module to increase capabilities of railway control systems in highly automated train operations
Real Time Systems,
59(4), 636-661, 2023, DOI: https://doi.org/10.1007/s11241-023-09401-5

M. Al-Shanawani, A. B. Gok, A. Costanzo, D. Masotti, A. Moriconi, T. Salmon Cinotti

Efficient Telepowering Unit for Balise Transmission Modules Using Class-E Amplifier,
Submitted to: *IEEE Transactions on Transportation Electrification*, Currently undergoing peer review

International conference papers

M. Barbareschi, S. Barone, V. Casola, P. Montone, A. Moriconi,
A Memory Protection Strategy for Resource Constrained Devices in Safety Critical Applications
2022 6th International Conference on System Reliability and Safety (ICSRS),
Venice, Italy, Oct. 2022, pp. 533-538, IEEE, DOI: 10.1109/ICSRS56243.2022.10067350

G. Mezzina, A. Amendola, M. Barbareschi, S. De Simone, G. Mascellaro, A. Moriconi, C. L. Saragaglia, D. Serra, D. De Venuto
A Step Toward Safe Unattended Train Operations: A Pioneer Vital Control Module.
2023 Design, Automation & Test in Europe Conference & Exhibition (DATE)),
Antwerp, Belgium, Apr. 2023, pp. 1-4, IEEE, DOI: 10.23919/DATE56975.2023.10137186

G. Mezzina, C. L. Saragaglia, M. Barbareschi, D. Serra, S. De Simone, A. Moriconi, D. De Venuto
Model-Based Vital Control Architecture for Highly Automated Train Operations*2022*
International Conference on Applications in Electronics Pervading Industry, Environment and Society
Genova, Italy, Sept. 2023, pp. 163-170, Springer Nature Switzerland, DOI: https://doi.org/10.1007/978-3-031-30333-3_21

Research products

- Awards:
  - The International conference paper “A Memory Protection Strategy for Resource Constrained Devices in Safety Critical Applications” has been selected as the best of his session at the the 2022 6th International Conference on System Reliability and Safety (ICSRS 2022) held during November 23-25, 2022 in Venice, Italy.

- Approximate computing tools:
  - pyALS -Python implementation of the catalog-based Aig-rewriting approximate Logic Synthesis technique
  - yosys-als: A design space exploration tool for approximate circuits
  - Soon to be published: luta-livre

PhD thesis overview

- The problem we tackled is that, while approximate variants of circuits can provide important performance savings, obtaining them can be hard
- Objective

  Our objective has been to devise an automatical mehtodology and tool to enable a designer to obtain multiple approximate variants of a circuit described in a HDL
- Methodology

  Our exploration started with the idea of "optimally solving" the problem of approximation for "small circuits", and tackling design space exploration for bigger circuits as a multi-objective optimization problem

Exact Approximate Synthesis

- Our first contribution comprises a description of the problem of providing a variant for «small circuits» (i.e. up to 6 inputs, a single output) in terms of hamming distance between specifications
- The question is: what's the best circuits that only gives the incorrect output for «up-to n» input vectors?
- The problem has been described as a SMT problem

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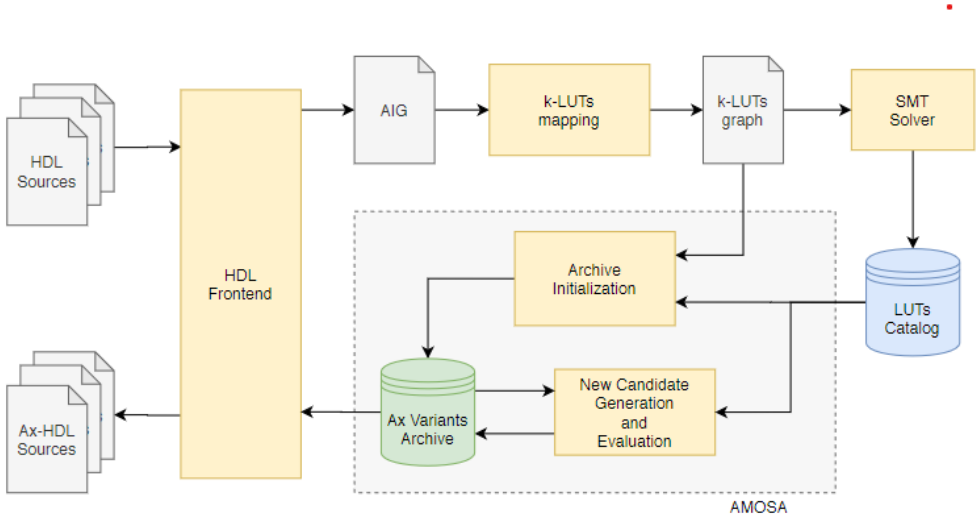
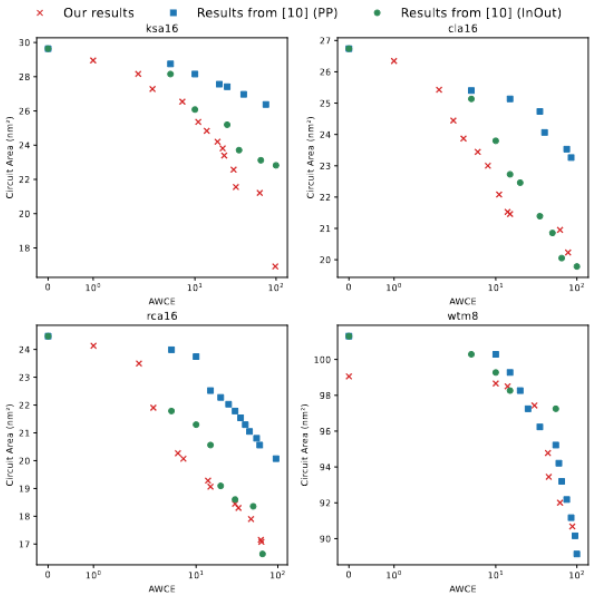
The rewriting methodology

- We applied this approach to selected cuts of the circuit AIG representation
- We then apply a multi-objective optimization algorithm to obtain an estimate of the Pareto frontier according to selected error and performance metrics

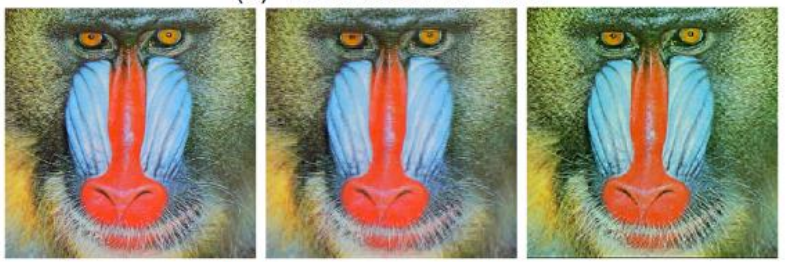


Benchmarking and case studies

- We benchmarked our methodology against industry-standard circuit synthesis test suites
- We show improvements w.r.t. state of the art approximate circuit synthesis methodologies



(a) Visual test with Lena



(b) Visual test with Baboon

Observations

- While various error metrics are used, we optimize for circuit area because there's a direct correlation between the number of the nodes in the AIG representation and the resulting circuit area on ASIC technology

Bridging our results to FPGA

- Before devising a new methodology, we wanted to understand if we would be able to replicate the results on FPGA technology (Xilinx Series 7)
- We found that, while optimization for node count in AIG is «intuitively» an ASIC-related metric, the resulting circuits, after FPGA synthesis, show improvements both in circuit area and switching activity

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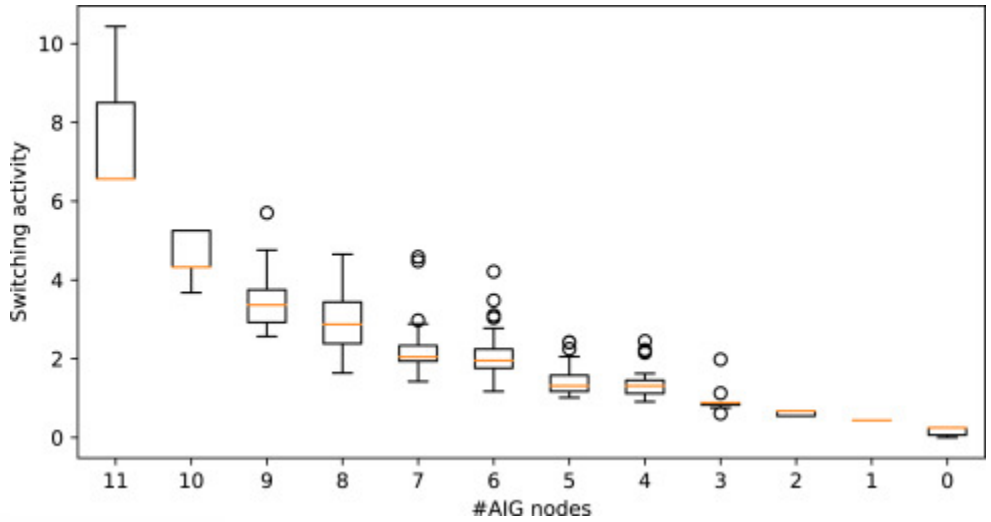
Bridging our results to FPGA

- We believe analitically briding AIG nodes and power dissipation is still an open problem
- Experimental findings based on a simple LUT power dissipation model however confirm the trend



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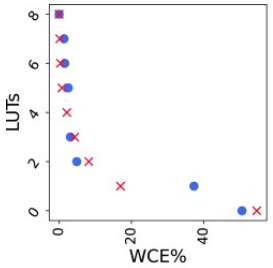
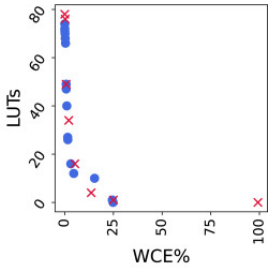
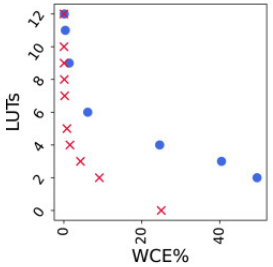


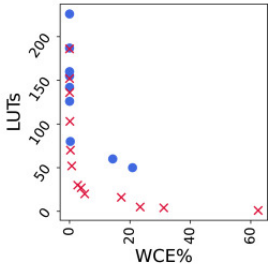
(a) unsigned 8-bits adder



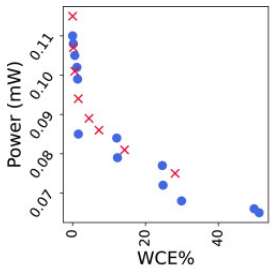
(b) unsigned 8-bits multiplier



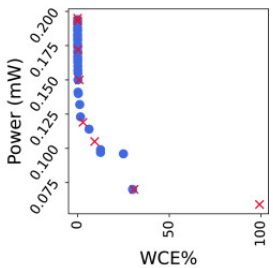
(c) unsigned 12-bits adder



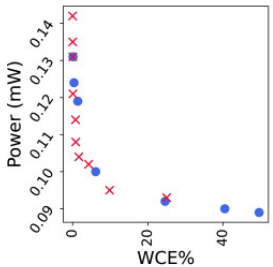
(d) unsigned 12-bits multiplier



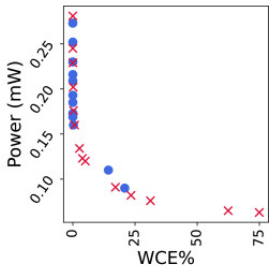
(a) unsigned 8-bits adder



(b) unsigned 8-bits multiplier



(c) unsigned 12-bits adder



(d) unsigned 12-bits multiplier

Benchmarking and case studies

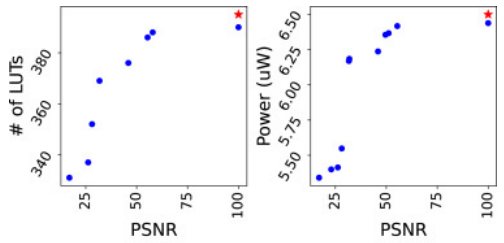
- We also used our circuits in some practical applications, such as Sobel filters, FIR filters and CNN accelerators

Sobel

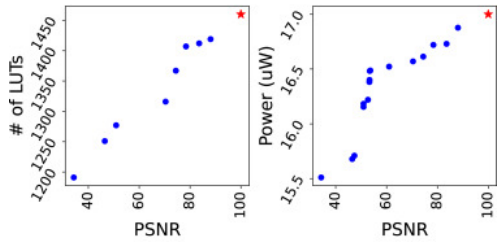
(a) Visual test with Pepper

(b) Visual test with House

FIR

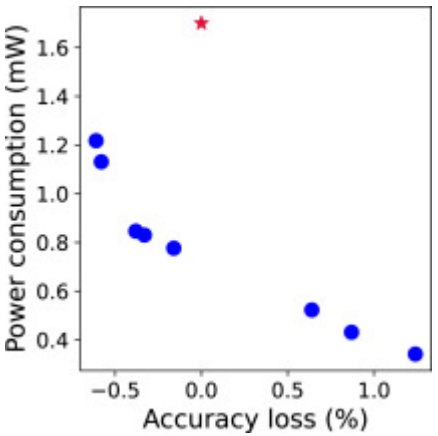


(a) 8-bits FIR



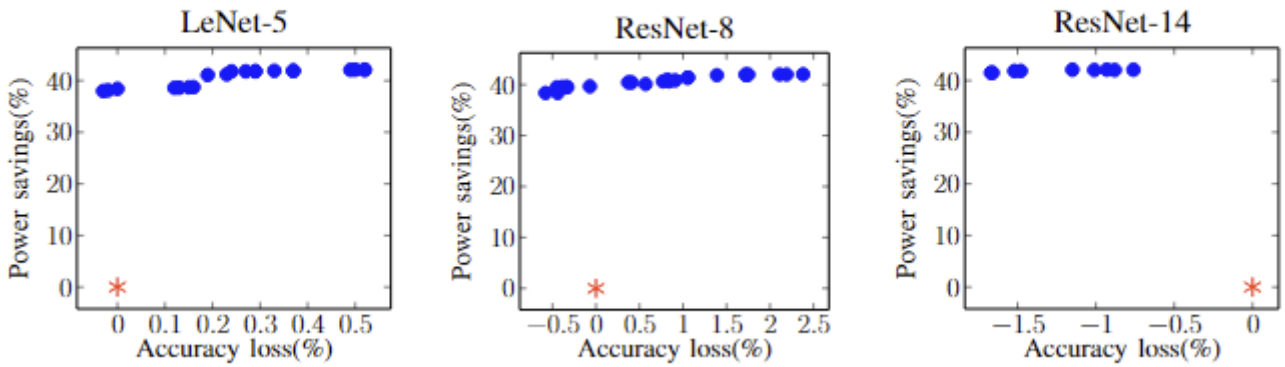
(b) 16-bits FIR

LeNet5



Leveraging FPGA specific approaches

- By implementing a very fast power dissipation estimation model we have been able to use switching activity as the optimization metric, thus obtaining even better results



Leveraging FPGA specific approaches

- Our latest tool, luta-livre, for which an experimental campaign is still undergoing, approaches the problem from a FPGA specific point-of-view
- Power dissipation estimation models are applied locally instead of exact synthesis, and candidate LUT specifications are chosen based on probability of inputs
- When targeting arithmetic circuits, a boolean polynomial difference approach has been used to quickly evaluate circuit error