PhD in Information Technology and Electrical Engineering
Università degli Studi di Napoli Federico II

PhD Student: Marco Boccarossa

Cycle: XXXVII

Training and Research Activities Report

Academic year: 2022-23 - PhD Year: Second

Tutor: prof. Andrea Irace

Co-Tutor: prof. Luca Maresca

Date: October 31, 2023

Training and Research Activities Report

PhD in Information Technology and Electrical Engineering

Cycle: XXXVII **Author: Marco Boccarossa**

1. Information:

- **PhD student: Marco Boccarossa** **PhD Cycle: XXXVII**
- **DR number: DR995862**
- **Date of birth: 02/06/1995**
- **Master Science degree: Electronic Engineering** **University: Federico II**
- **Scholarship type: DIETI**
- **Tutor: prof. Andrea Irace**
- **Co-tutor: prof. Luca Maresca**

2. Study and training activities:

Activity	Type[1]	Hours	Credits	Dates	Organizer	Certificate[2]
SSM Scientific Colloquia (1)	Seminar	1	0.2	10/11/2022	Dr. M. Benetti, Dr. M. Coraggio	N
SSM Scientific Colloquia (2)	Seminar	1	0.2	17/11/2022	Dr. M. Benetti, Dr. M. Coraggio	N
From Cyber Situational Awareness to Adaptive Cyber Defense: Leveling the Cyber Playing Field	Seminar	2	0.4	13/12/2022	Prof. Massimiliano Albanese	N
SSM Scientific Colloquia (5)	Seminar	1	0.2	16/12/2022	Prof. Olivier Minazzoli	N
SSM Scientific Colloquia (6)	Seminar	2	0.4	12/01/2023	Prof. Valerio Cozzani	N
Open Digital Framework – Crash Course	Seminar	3	0.6	17/01/2023	Alberto Curcio	Y
Industry 4.0 Fundamentals in Bosch Applications	Seminar	10	2	23-26/01/2023	Prof. Mariagrazia Dotoli	Y
ITIL – Crash Course	Seminar	3	0.6	24/01/2023	Alberto Curcio	Y
Principi Architetturali - TOGAF I	Seminar	3	0.6	30/01/2023	Alberto Curcio	Y
Scientific Programming and Visualization with Python	Course	24	2	21-23/02/2023	Prof. Alessio Botta	Y
How To Boost Your PhD	Course	16	4	01/2023-04/2023	Dr. Antigone Marino	Y
Fulbrighters Fredericiani a Ingegneria	Seminar	2	0.4	26/06/2023	Prof. Giuseppe Ruello	N
SIE 2023	PhD School	20	4	04-06/09/202	Prof. Carmine Ciofi	Y

Fondi Europei e Programmazione 2021/2027	Course	2	0.4	14/09/2023	Dr. Tommaso Foglia	N
Panoramica delle Opportunità di Finanziamento	Course	3	0.6	28/09/2023	Dr. Tommaso Foglia	N

1) Courses, Seminar, Doctoral School, Research, Tutorship
2) Choose: Y or N

2.1. Study and training activities - credits earned

	Courses	Seminars	Research	Tutorship	Total
Bimonth 1	0	1	9	0	10
Bimonth 2	2	4.2	3.8	0	10
Bimonth 3	4	0	6	0	10
Bimonth 4	0	0.4	9.6	0	10
Bimonth 5	0	0	10	0	10
Bimonth 6	5	0	5	0	10
Total	**11**	**5.6**	**43.4**	**0**	**60**
Expected for II year	**10 - 20**	**5 - 10**	**30 - 45**	**0 – 1.6**	

3. Research activity:

Semiconductor electronic devices are crucial in power electronics applications for controlling and processing electric power. Silicon has been the dominant semiconductor in power electronics, but, as the market demands higher performance, robustness, and reliability, Silicon faces physical constraints. To address these issues and environmental concerns, wide bandgap (WBG) materials like Gallium Nitride (GaN) and Gallium Oxide (GaO) are gaining attention. Among these materials, Silicon Carbide (SiC) is the most mature and offers advantages like minimal switching losses and high switching frequencies. In designing and studying electronic power devices, Technology Computer Aided Design (TCAD) simulations play a critical role. TCAD simulators use finite element analysis to solve semiconductor equations and model semiconductor devices. They enable the prediction of device performance before physical fabrication, reducing development time and costs while allowing the investigation of physical phenomena within the device.

Study on fast recovery epitaxial Si diodes (in collaboration w/ Vishay Semiconductor Italia)
The need to optimize the design of silicon diodes has arisen due to the technological limits of silicon development. To support the Si diode market, it's crucial to manage trade-offs between on-state, off-state, and commutation performance. The active area of the diode, which supports current conduction during normal operation, is a key focus. Parameters like on-state voltage (V_{ON}) and commutation features, including peak reverse recovery current (I_{rr}), reverse recovery time (t_{rr}), reverse recovery charge (Q_{rr}), and snappiness factor (S), play a crucial role in evaluating diode performance. TCAD simulations are used to identify design variables controlling these parameters and find optimal trade-offs.

Calibration of the simulator was necessary, starting with electrical characterization of an existing device provided by a technological partner. This helped ensure the simulator's behavior was consistent with the actual device, enhancing predictive simulations. Subsequent simulations explored the effect of varying the active area design on device performance.
Modern power semiconductor devices are not only assessed based on their electrical properties but also their reliability. Ruggedness during avalanche conditions is essential and evaluated through the Unclamped Inductive Switching (UIS) test. The termination region design significantly impacts avalanche performance, preventing a lower breakdown voltage (V_{BR}) in the active region. Diodes must also be rugged against ElectroStatic Discharge (ESD), often caused by contact with the human body and simulated using the Human Body Model (HBM).
The overall objective is to generate a matrix of diverse designs for the active area, evaluated for conduction performance and reliability. This matrix will offer options suitable for various applications.

Study on design parameters of SiC diodes (in collaboration w/ Vishay Semiconductor Italia)
SiC diodes, specifically Schottky barrier diodes (SBDs), are well-established in the SiC semiconductor field. Unlike PiN diodes, SBDs are unipolar devices, which means they have a higher voltage drop at high currents. To mitigate this, current SiC diodes often incorporate regularly spaced p+-wells in their structure. These p+-wells reduce leakage current by moving the peak of the electric field away from the metal-semiconductor interface and may assist with current conduction during surge events. The resulting device is either a Junction Barrier Schottky (JBS) diode if the metal used for the anode contact inhibits p+-zone conduction or a merged PiN-Schottky (MPS) diode if the metal forms an Ohmic contact, allowing p+-zone conduction.
To ensure that the p+ implantation effectively aids forward conduction through minority injection, it is crucial to select the Schottky barrier height at the p+/metal interface carefully. This means that defining a single anode contact that behaves as Schottky when connected to n-regions and as Ohmic when connected to p-wells might be challenging.
The primary objective of this work is to establish a methodology for accurate MPS diode simulation, allowing for the assessment of how design parameters affect its electrical characteristics. Afterward, the research aims to explore how the active area design of SiC diodes impacts the device's static behavior.

Compact models for mixed mode simulations
Diodes are integral components within complex electronic circuits. After simulating diode behavior with TCAD simulations, it's important to understand how they interact with other circuit components. However, creating physical models for every single electronic component is impractical due to the significant simulation time required. To address this challenge, mixed-mode simulations are employed, which involve simulating the physical model of the target device alongside compact models.
TCAD simulators offer simple compact models compatible with passive components like resistors, capacitors, or inductors. However, for active components such as MOSFETs, the embedded compact models may not provide sufficient accuracy.
The main objective of this work is to tackle this issue by developing a compact model for a commercial SiC MOSFET that is compatible with TCAD's physical models. This allows for rapid yet accurate simulations. Specifically, existing compact models from manufacturers aren't directly compatible with TCAD simulations, so a behavioral model is created using a C++ interface. This approach enables the use of the newly created compact model in combination with the simulator's provided compact models

to simulate the behavior of the target device within complex circuits and obtain accurate results in a reasonable amount of time.

Improvement of the Short-Circuit Capability of SiC MOSFETs (in collaboration w/ Ca' Foscari University of Venice)
Silicon Carbide (SiC) power MOSFETs are gaining popularity in the industry as a compelling alternative to traditional silicon-based power MOSFETs. This shift is due to their superior performance characteristics, including higher breakdown voltage, faster switching speeds, and lower on-resistance. These advantageous properties make SiC power MOSFETs competitive in various medium and high-voltage applications, such as automotive, aerospace, renewable energy distribution, and more.
A well-engineered device should not only perform efficiently during standard operation but also endure demanding abnormal conditions. To evaluate the reliability of a SiC power MOSFET design, a widely used validation test is the short-circuit (SC) test. Since the failure occurrence during a SC event is strongly linked to the temperature increase, TCAD simulations show how using a non-linear dielectric, characterized by a temperature-dependent permittivity (ε), mitigates the temperature dependence of the drain current, reducing the maximum temperature rising into the device and improving its ruggedness in SC.

4. Research products:

- **M. Boccarossa**, L. Maresca, A. Borghese, M. Riccio, G. Breglio, A. Irace, and G. A. Salvatore, "Short-Circuit Rugged 1.2 kV SiC MOSFET with a Non-Linear Dielectric Gate Stack," *2023 35th International Symposium on Power Semiconductor Devices and ICs (ISPSD)*, Hong Kong, 2023, pp. 354-357, doi: 10.1109/ISPSD57135.2023.10147604.
- V. d'Alessandro, V. Terracciano, A. Borghese, **M. Boccarossa**, and A. Irace, "A Simple Electrothermal Compact Model for SiC MPS Diodes Including the Snapback Mechanism," *2023 29th International Workshop on Thermal Investigations of ICs and Systems (THERMINIC),* Budapest, Hungary, 2023. *(in press)*
- **M. Boccarossa**, L. Maresca, A. Borghese, M. Riccio, G. Breglio, A. Irace, and G. A. Salvatore, "Threshold Voltage Temperature Dependence for a 1.2 kV SiC MOSFET with Non-Linear Gate Stack*," 2023 International Seminar on Power Semiconductors (ISPS) Proceedings*, Czech Technical University in Prague, Czech Republic, 2023. *(in press)*
- **M. Boccarossa**, L. Maresca, A. Borghese, M. Riccio, G. Breglio, A. Irace, and G. A. Salvatore, "Non-Linear Gate Stack Effect on the Short Circuit Performance of a 1.2-kV SiC MOSFET," *2023 20th International Conference in Silicon Carbide and Related Materials (ICSCRM),* Sorrento (NA), Italy, 2023. *(in press)*
- A. Borghese, S. Angora, **M. Boccarossa**, M. Riccio, L. Maresca, V. R. Marrazzo, G. Breglio and A. Irace, "Analysis of Electrothermal Imbalance of Hard-Switched Parallel SiC MOSFETs Through Infrared Thermography," *2023 20th International Conference in Silicon Carbide and Related Materials (ICSCRM),* Sorrento (NA), Italy, 2023. *(in press)*
- L. Maresca, V. Terracciano, A. Borghese, **M. Boccarossa**, M. Riccio, G. Breglio, A. Mihaila, G. Romano, S. Wirths, L. Knoll, and A. Irace, "SiC GAA MOSFET concept for high power electronics performance evaluation through advanced TCAD simulations," *2023 20th International Conference in Silicon Carbide and Related Materials (ICSCRM),* Sorrento (NA), Italy, 2023. *(in press)*

- V. Terracciano, A. Borghese, **M. Boccarossa**, V. d'Alessandro, and A. Irace, "A Geometry-Scalable Physically-Based SPICE Compact Model for SiC MPS Diodes Including the Snapback Mechanism," *2023 20th International Conference in Silicon Carbide and Related Materials (ICSCRM),* Sorrento (NA), Italy, 2023. *(in press)*

5. Conferences and seminars attended

- *35th IEEE International Symposium on Power Semiconductor Devices and ICs (ISPSD 2023),* SHAW Auditorium, Hong Kong University of Science and Technology (HKUST), Hong Kong, 28 May – 01 June 2023, **poster presentation.**
- *16th International Seminar on Power Semiconductors (ISPS 2023),* Czech Technical University in Prague, Czech Republic, 30 August – 01 September 2023, **oral presentation.**
- *PhD School Società Italiana di Elettronica (SIE 2023): "How Electronics drives global innovation",* Messina, Italy, 04 – 06 September 2023
- *54th annual Meeting of the Società Italiana di Elettronica (SIE 2023*), Noto (SR), Italy, 06 – 08 September 2023, **poster presentation.**
- *20th International Conference on Silicon Carbide and Related Materials (ICSCRM 2023),* Sorrento (NA), Italy, 17 – 22 September 2023, **poster presentation.**

6. Periods abroad and/or in international research institutions

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7. Tutorship

- 47-hour tutorship assistance to 2nd year course *"Metodi Matematici per l'Ingegneria".*

8. Plan for year three

For the third year, I plan to continue my research on the design and development of power semiconductor devices based on wide-bandgap materials, delving deeper into the use of ferroelectric materials in power electronics.
Moreover, I plan to spend six months abroad at the University of Warwick, Coventry, UK, where I will go into detail in the fabrication process of semiconductor power devices.