Marco Vitone

Development of innovative techniques and methodologies for analysis and testing of Storage Systems interfaces based on System on Chip

Tutor: Prof. Nicola Petra

co-Tutor: Ing. Claudio Giaccio

Cycle: XXXVI

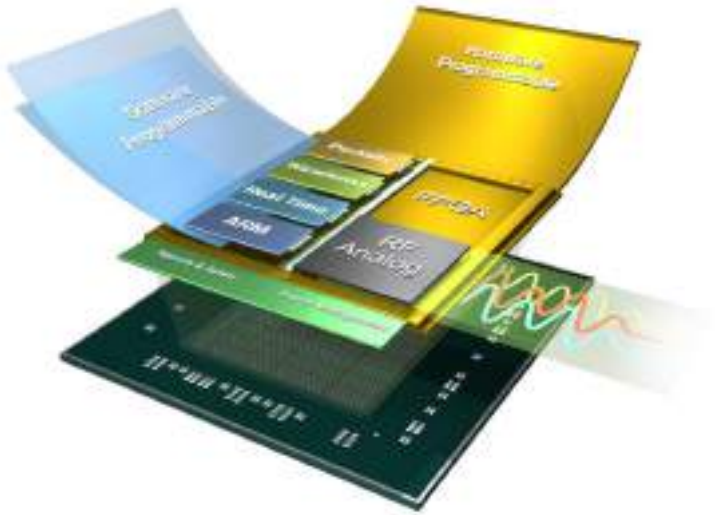
Year : 1

My background

- MSc degree in Electronics Engineering
- Research group/laboratory : VLSI Elctronics
- PhD start date : 1/11/2020
- Scholarship type: founded by Micron Semiconductor Italia S.R.L.
- Cooperation : Micron Hardware Validation Tool Team

Research field of interest

- System on Chip is a complex IC that integrates CPU, on-chip memory, programmable logic (FPGA) on a single chipset.



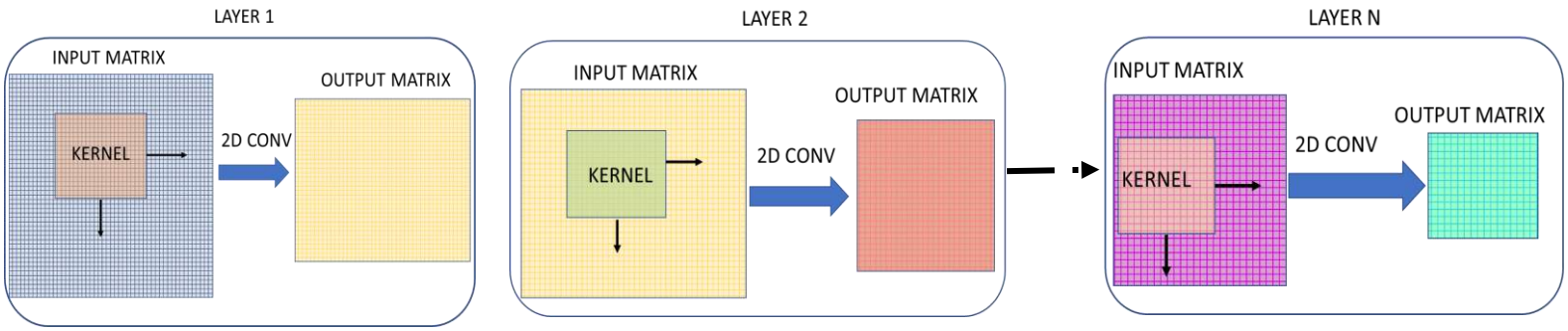
- My research focuses on
  - **Design** of SoC:
    - **Implementation of hardware accelerator**
    - **Validation and Debug** of SoC adopting Universal Verification Methodology (UVM)

Summary of study activities

- Ad hoc PhD courses
  - Digital Forensics' method, practices and tools
  - Statistical data analysis for science and engineering research
  - Data Science for Patient Record Analysis
  - Scientific Programming and Visualization with Python
  - Imprenditorialità accademica
  - Strategic Orientation for STEM Research & Writing
- PhD School
  - Electronics for IoT (SIE 2021)
- Courses attended borrowed from MSc curricula
  - Dispositivi e sistemi fotovoltaici
- Conferences / events attended
  - SIE 2021, 52nd Annual Meeting of Associazione Società Italiana di Elettronica

Research activity: Overview

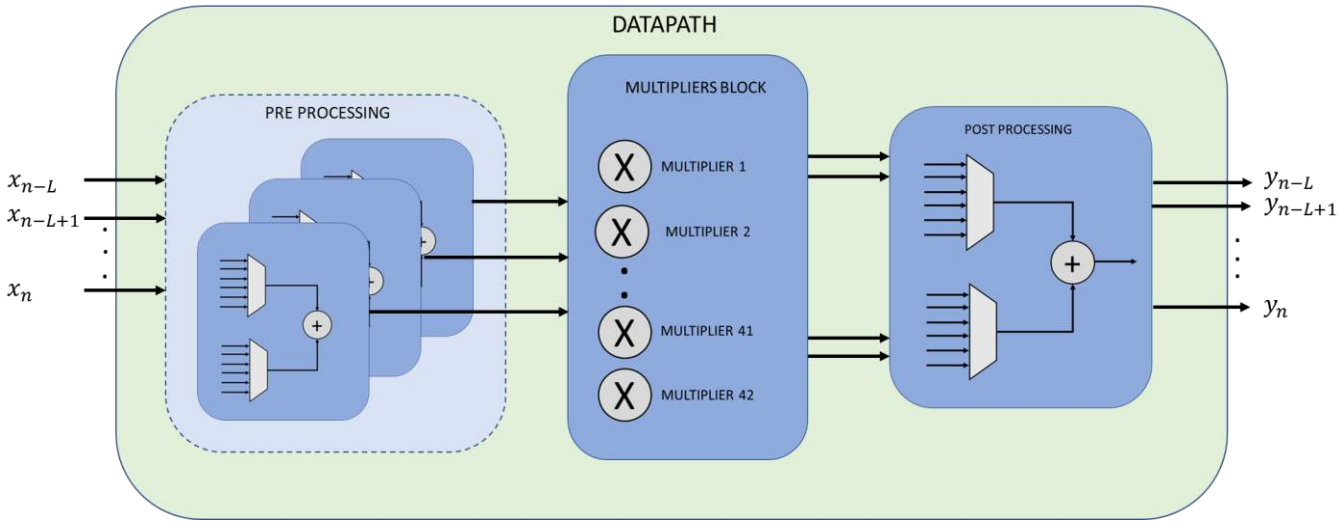
- Problem
  - Convolutional Neural Network
  - Convolutions require a huge number of multiplications thus decreasing performance in software applications



- Objective
  - Development of algorithm to reduce the overall number of multiplications needed
  - Hardware acceleration of CNN through SoC data-path

Research activity: Overview

- Intended contribution (in perspective)
  - Novel k-parallel fast finite impulse response algorithm (FFA)
  - Design of reconfigurable data-path on SoC for hardware acceleration of computations performed in CNN

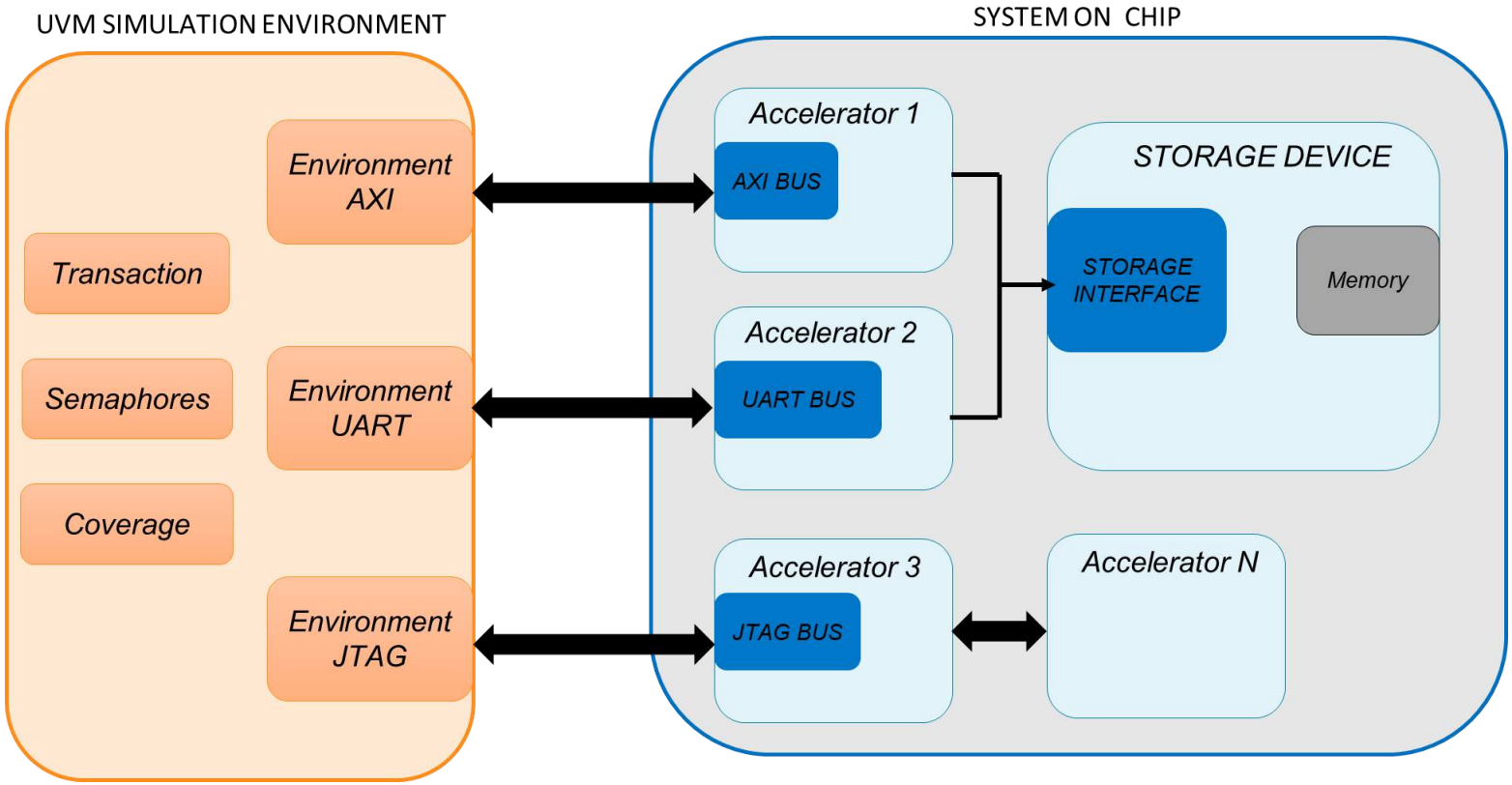


Research activity: Overview

- Problem
  - SoC integrates a wide variety of components:
    - Processors
    - Hardware accelerator
    - Storage Interface (UFS, eMMC)
    - Bus interface (AXI, UART,JTAG and so on)
  - Thus, the validation and debug of SoC became challenging.

- Objective
  - Development of simulation environment for complex SoC
  - Usage of UVM technique improving reusability, robustness and simulation coverage

Research activity: Overview



Research activity: Overview

- Intended contribution (in perspective)
  - Development UVM simulation environment for a complex SoC in collaboration with Micron Team.
  - First achievement:
    - Improvement of the overall performance respect to the previous Micron custom simulation environment
    - Reduction of the simulation time : **about 50%.**

PREVIOUS SIMULATION ENVIRONMENT

- Number of tests executed : **53**
- Simulation time consumption: **9h 34m**

PROPOSED SIMULATION ENVIRONMENT

- Number of tests executed : **106**
- Simulation time consumption: **10h 11m**

Products

[C1]	Vitone, M.; Petra,N. *"Reconfigurable Datapath for Hardware Acceleration of Convolutional Neural Network"* SIE-2021, 52nd Annual Meeting of Associazione Società Italiana di Elettronica

	Courses	Seminars	Research	Tutorship	Total
Bimonth 1	3	3.2	4	0	10.2
Bimonth 2	9	3	2	0	14
Bimonth 3	8.5	3.9	2	0	14.4
Bimonth 4	0	0.6	8	0	8.6
Bimonth 5	7.4	0	1.6	0	9
Bimonth 6	4	0	6	0	10
Total	31.9	10.7	23.6	0	66.2
Expected	30 - 70	10 - 30	80 - 140	0 – 4.8	

Thanks for the attention !