PhD in Information Technology and Electrical Engineering
Università degli Studi di Napoli Federico II

PhD Student: Gerardo Saggese

Cycle: XXXVI

Training and Research Activities Report

Academic year: 2021-22 - PhD Year: Second

Gerardo Saggese

Tutor: prof. Antonio G.M Strollo

Date: October 30, 2022

1. Information:

- **PhD student: Gerardo Saggese** **PhD Cycle: XXXVI**
- **DR number: 995145**
- **Date of birth: 20/04/1995**
- **Master Science degree: Double Degree in Electronic Engineering and in Electronics and Telecommunications**
- **University: University of Napoli Federico II and Technical University of Lodz**
- **Scholarship type: MIUR-PRIN 2017**
- **Tutor: prof. Antonio G.M Strollo**

2. Study and training activities:

Activity	Type[1]	Hours	Credits	Dates	Organizer	Certificate[2]
Vehicular Hacking in Akka Tecnologies	Seminar	1.5	0.3	3/11/21	Dr. L.Guido	Y
Cyber security in Akka Tecnologies	Seminar	2	0.4	3/11/21	Dr. L Villa	Y
Exploring the early Universe through the cosmic microwave background	Seminar	1.5	0.3	4/11/21	Pr. P. Notoli	Y
Evolution by curvature of networks in the plane	Seminar	1	0.2	11/11/21	Prof. C. Montegozza	Y
Turbolent Dynamics in viscous fluids: a complex phenomenon ubiquitous in nature	Seminar	1.5	0.3	18/11/21	Prof. V. Carbone	Y
Graphons: a tool for the analysis of the systems on large networks	Seminar	1	0.2	25/11/21	Dr. P. Frasca	Y
Connecting the dots: Investigating an APT compaign using Splunk",	Seminar	2	0.4	26/11/21	Dr. A. Forzieri	Y

Threat Hunting Essentials	Seminar	2	0.4	3/12/21	Group-IB	Y
Threat Hunting Use-Cases	Seminar	2	0.4	13/12/21	Group-IB	Y
GDPR basics for computer scientists	Seminar	2	0.4	14/12/21	Dr. R. Wenning	Y
All roads lead to WebRTC	Seminar	2	0.4	16/12/21	Dr. L. Miniero	Y
Design Quantum algorithms	Seminar	2	0.4	16/12/21	Pr. M. Amoretti	Y
Social network dynamics leading to community formation and residential segregation	Seminar	1.5	0.3	16/12/21	Prof. M. Franceschetti	Y
Structure, processes and dynamics of networks with higher order interactions	Seminar	1.5	0.3	13/01/22	Dr. S. Boccaletti	Y
The needle in the haystack: the search for rare processes and the fundamental laws of Nature	Seminar	1.5	0.3	17/02/22	Pr. F. Ambrosino	Y
An overview of the transient sky at high energies	Seminar	1.5	0.3	3/03/22	Dr. Anrea Sanna	Y
Global and cluster synchronization in complex networks and beyond	Seminar	1.5	0.3	10/03/22	Pr. M. Frasca	Y
High Energy X-ray Astrophysics from Space revealing the backbones of the Universe	Seminar	1.5	0.3	17/03/22	Pr. M. Paolillo	Y

From basic principles in spintronics to some recent developments toward spinorbitronics	Seminar	1.5	0.3	31/03/22	Dr. V. Cros	Y
Capillary Surfaces and a Model of Nanowire Growth	Seminar	1.5	0.3	7/04/22	Pr. M. Morini	Y
FPGA per l'elaborazione dei segnali	MSc Course	72	9	30/03/22-7/06/22	Pr. N. Petra	Y
Ultra-low power integrated systems for green growth to the trillion scale	Ph.D Course (Uni. Pisa)	16	4	20/06/22-22/06/22	Pr. M. Alioto	Y
An informal discussion around stochastic and freeboundary problems	Seminar	1.5	0.3	12/05/22	Dr. L. Buoninfante	Y
Are 2 derivative enough to describe nature at a fundamental level	Seminar	1.5	0.3	19/05/22	Pr. T. de Angelis	Y
Impreditorialità Accademica	Ad hoc Course	20	4	26/05/22-26/07/22	Pr. P. Rippa	Y
Biosignals measurement and analysis	Ad hoc Course	20	4	15/06/22-13/07/22	Dr. E. Andreozzi	Y
Ph.D School "Automotive Electronics"	Doc. School	16	4	5/09/22-7/09/22	Pr. Felice Crupi	Y
Comprehensive Digital IC Implementation & Sign-Off	Seminar	35	7	3/10/22-5/10/22	Europractice	N

1) Courses, Seminar, Doctoral School, Research, Tutorship
2) Choose: Y or N

2.1. Study and training activities - credits earned

	Courses	Seminars	Research	Tutorship	Total
Bimonth 1	**0**	**4.4**	**6.5**	**0**	**10.9**
Bimonth 2	**0**	**0.6**	**6.5**	**0**	**7.1**
Bimonth 3	**0**	**1.5**	**6.5**	**0**	**8**
Bimonth 4	**13**	**0.6**	**6**	**0**	**19.6**
Bimonth 5	**8**	**0**	**5**	**0**	**13**
Bimonth 6	**4**	**7**	**6**	**0**	**17**
Total	**25**	**14.1**	**36.5**	**0**	**75.6**
Expected	**30 - 70**	**10 - 30**	**80 - 140**	**0 – 4.8**	

3. Research activity:

My research interest focuses on brain-machine interfaces (BMIs) (study, analysis, and implementation of spike detection algorithms) as well as approximating computing for low-power and error-resilient hardware architectures.

BMIs:

Brain-machine interfaces (BMIs) are nowadays considered one of the most effective tools to study brain activity, using the recording and the analysis of action potentials, described as a boost of instantaneous energy, or, briefly, spikes. Breakthroughs in recording technology have increased the number of recorded neurons and provided better signal quality. Development of BMI-based devices, however, faces several challenges: the integration of the entire system in a small-physical size chip, the high-speed functionality to support the real-time streaming of neural activities, the limited bandwidth offered by the wireless channel, the need to transmit a huge amount of data, and the limited power offered by battery or harvesting system. On-implant signal processing becomes essential to reduce the bandwidth to make it possible for wireless transmission, and, for that, spike detection algorithms have received intensive attention from the field of neurophysiology, due to their capabilities of reducing the massive amount of data recorded by neural devices. In such a way, by sending only useful information, the communication bandwidth can be reduced from tens of MB/s to a few kB/s. Then, an off-chip post-processing elaboration is exploited to verify and sort the extracted spikes without any power and performance constraints.
A standard workflow of spike detection includes a filtering stage to reduce out-of-band noise, a spike enhancement block, followed by thresholding for spike identification and extraction. The threshold can be either constant or adaptive, to ensure an acceptable compromise between false positives (noise wrongly detected as a spike) and false negatives (a spike being discarded). Several methods and operators have been proposed to increase the signal-to-noise ratio (SNR), by enhancing the spikes with respect to the background noise. A popular class of data compression techniques is based on non-linear operators, like Non-linear Energy Operator (NEO), Amplitude Slope Operator (ASO), and their variants, which are meant to be sensitive to energy signal variations. By describing a spike as a short-lived burst with high amplitude and frequency, these operators increase the differentiation between spikes and noise, enhancing the SNR. This characteristic, together with a great trade-off between computational cost and accuracy, makes them more amenable to real-time data reduction goals. Additionally, extracellularly recorded signals are inevitably corrupted by noise from several sources: the recording hardware, electromagnetic interference, the superimposed activity of multiple neurons, and the spatially averaged activity of distant neurons. Importantly, the activity of distant neurons appears as noise which is highly correlated with the signal of interest (Local Field Potentials), described as a low-frequency oscillation. Further, the shape and amplitude of the signals of interest are highly variable. Thus, the design of the threshold constitutes another challenging task. It should adapt to different noise scenarios and to different spike firing rates over time.

In [**1-j**] we investigate and propose a new spike detector based on the novel energy operator called ASO together with a novel noise estimate addressed as WA based on mean-clipped

operation and cyclically used to update the threshold level. The algorithm was initially developed in MATLAB using floating-point arithmetic and testing detection performance by using both synthetic and real data. A 1024 multi-transistor arrays (MTAs) very large-scale integration (VLSI) architecture is also provided to demonstrate hardware efficiency, real-time capability, and power requirements by means of the integration/design of a static random-access memory (SRAM) based on latches. We show that the novel non-linear energy operator called ASO in combination with a simple but robust noise estimate achieves a good trade-off between performance and consumption. The final architecture (1024 channels) occupies an area of 2.3 mm^2, dissipating 3.6 µW per channel. The comparison with the state of the art showed that our proposal finds a place among other methods presented in the literature, certifying its suitability for BMIs.

In [**2-c**], we started to investigate the possibility of a multi-resolution non-linear energy operator, finding in the cascade of ASO and ADO (amplitude differential operator) the one that gives the best performance-accuracy trade-off. This allowed us to avoid the integration of a smoothing window that has been demonstrated to challenge the multichannel implementation constraints even when an equivalent filter was used [**1-j**]. In this work, a newer noise estimate was also investigated based on the conjunction of mean square and three-point medina operator to discard the outlier into the noise distribution (e.g, spikes). A single-channel spike detector based on such features was designed and demonstrated to be competitive with the state of the art of brain-machine interfaces. A further analysis is conducted in [**5-j**]. This work is an extension of [**2-c**], where we further investigate the operators cascade together with a simple and fully adaptive threshold. Based on the proposed technique, a 1024-channel neural signal processor is also designed in a 28 nm TSMC CMOS process by using latch-based static random-access memory (SRAM), demonstrating a total power consumption of 1.4 µW/ch and a silicon area occupation of 230 $µm^2$/ch. These features, together with a comparison with the state of the art, demonstrate that our proposal constitutes an alternative for the development of next-generation multichannel neural interfaces.

Approximating Computing:

The ever-lasting demand for power and speed improvement has driven researchers, towards approximate computing. Approximate computing is a fast-emerging field in digital design that sacrifices the exactness of computations over significant improvement in power dissipation, speed, and circuit area. Such techniques can be utilized in cloud computing, embedded and mobile devices, where high speed and power minimization are important constraints. Approximate computing finds fertile soil in error-resilient applications such as multimedia processing, data mining and recognition, and machine and deep learning.
Concerning approximate computing, a plethora of studies has focused on arithmetic operations, such as binary addition, multiplication, and division. Nowadays approximate binary multipliers are being studied thoroughly. Several techniques providing efficient approximate multipliers have been proposed in the literature.

An important class of approximate multipliers, dubbed segmented multipliers, extracts a set of m contiguous bits (an m-bit segment) from each of the two n-bit operands, uses an inner

m × m multiplier to multiply the two segments, and expands the 2m-bit multiplication to the final 2n-bit result. In a Static Segmented Multiplier (SSM), the operands are statically split into two m-bit segments. This approach greatly simplifies hardware implementation, reducing power consumption, since leading-one detectors and shifters are not required. On the other hand, for the same inner m × m multiplier, static segmentation results in larger errors compared to dynamic segmentation. In [**2-j**] we perform a detailed analysis of SSMs and propose some improvements to the basic architecture and developed a novel segmentation technique for signed. Our circuits, compared to previously prosed approximate multipliers, provides very good error-electrical performance trade-off. We also investigated the performance of approximate multiplier in image filtering and image recognition applications. Obtained results confirmed that SSMs are good candidates in applications where their error performance is acceptable.
Customized approximate multipliers for efficient implementation of multiply-accumulate (MAC) blocks is also studied and designed in [**6-j**] by exploiting the static segmentation of our previous work. A naive approach of designing a SSMAC is cascading an adder to a static segmented multiplier. This approach is however ineffective since the original SSM uses a shifter to obtain the approximate product. Thus, including an adder after the shifter would result in the cascade of two carry-propagate additions (one to calculate the approximate product A×B, and one to sum C). The proposed SSMAC, on the contrary, is based on the merge of the multiplier and an adder in an unique approximate structure and performs segmentation not only on A and B, but also on operand C, to further reduce hardware cost. The proposed circuit can be configured at design-time by two parameters. The first one controls the segmentation on A and B, while the second one controls the segmentation on C and the adder length. Like [**2-j**], the SSMAC includes a compensation term to reduce the approximation error. Analysis of error metrics, synthesis results in 28 nm CMOS technology, and results from image processing applications validate our proposal.
The above works deal with fixed-point multipliers which have been extensively studied, but in recent years approximating computing techniques have been also introduced in floating-point multipliers to again save power and area, at cost of introducing some (small) errors in the results. Inspired by that, in [**4-j**] we proposed the design of a novel approximate static segmented floating-point multiplier (SSFPM) with static segmentation applied to the mantissa product. Mainly designed for a single precision format. To further improve performance, we introduced a novel segmentation-and-truncation approach which allowed us to eliminate the shifter normally present at the output of the segmented multiplier together a simple correction term for reducing the approximation error. The accuracy of the SSFPM can be accurately tailored at the design time, by acting on a single parameter. Analysis of the error metrics shows that the proposed SSFPM is competitive with the state-of-the-art. The power consumption and the area occupation, obtained by the synthesis in TSMC 28 nm CMOS technology, demonstrate remarkable performance. Finally, the results of signal processing applications such as JPEG compression, image filtering, and tone mapping of high dynamic range (HDR) images show the effectiveness of the proposed SSFPM.

The basic binary multiplication process can be divided into three parts: partial product generation, partial product reduction and carry-propagate addition. Approximate computing can be introduced in all these steps. Recursive multipliers are an interesting research area of

the approximate computing field that aims to use small elementary approximate multiplier blocks, suitably assembled, to design larger multipliers. The advantage of the recursive building of larger multipliers is that it avoids a dedicated design for every bit width and gains in terms of generality of the proposed approaches. We proposed two novel 4×4 approximate designs with minimal power requirements and competitive error performance, in [**1-c**,**3-j**]. The output is calculated by exploiting proper carry truncation and compensation techniques. These designs, along with an OR-based and an exact 4×4 multiplier, are used to generate 8x8 approximate multipliers. We have synthesized the circuits developed in this paper as well as various previously proposed contributions, using a commercial 14nm FinFET library. Syntheses show that our circuits, compared to previously proposed designs, provide good error-electrical performance trade-off. Obtained results confirm that our proposals are good competitors in error-resilient applications (image-processing and convolutional neural network). By exploiting the recursive approach, we also designed a squarer multiplier [**7-j]**. This work proposes a novel approximate binary squarer, obtained by recursively exploiting 4-bit approximate multipliers and squarers. The final designs cover a wide range of computing precision, providing the user with multiple choices of different cost vs. accuracy trade-offs. The proposed circuits, as well as competitive designs, are synthesized targeting a 14nm FinFET technology to determine the electrical characteristics. It has shown that the proposed squarers outperform the state-of-the-art in terms of power vs. precision. Compared to the exact 8-bit squarer, the least dissipative proposal reduces silicon area by 76%, power consumption by 71%, and minimum delay by 72%. The same circuit dissipates 2.4% less power than the least dissipative design found in literature, while providing 34% more accurate results. The behaviour of the considered designs is also tested in common error resilient applications, like signal demodulation and image processing.

4. Research products:

Journal contributions:

1.j - **G. Saggese** and A. G. M. Strollo, “A Low Power 1024-Channels Spike Detector Using Latch-Based RAM for Real-Time Brain Silicon Interfaces,” Electronics, vol. 10, no. 24, p. 3068, Dec. 2021, doi: 10.3390/electronics10243068.

2.j - A. G. M. Strollo, E. Napoli, D. De Caro, N. Petra, **G. Saggese** and G. Di Meo, "Approximate Multipliers Using Static Segmentation: Error Analysis and Improvements," in IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 69, no. 6, pp. 2449-2462, June 2022, doi: 10.1109/TCSI.2022.3152921.

3.j - E. Zacharelos, I. Nunziata, **G. Saggese**, A. G. M. Strollo and E. Napoli, "Approximate Recursive Multipliers Using Low Power Building Blocks," in IEEE Transactions on Emerging Topics in Computing, vol. 10, no. 3, pp. 1315-1330, 1 July-Sept. 2022, doi: 10.1109/TETC.2022.3186240.

4.j - G. Di Meo, **G. Saggese**, A. G. M. Strollo, D. De Caro, and N. Petra, “Approximate Floating-Point Multiplier based on Static Segmentation,” Electronics, vol. 11, no. 19, p. 3005, Sep. 2022, doi: 10.3390/electronics11193005.

5.j - **G. Saggese** and A. G. M. Strollo, "Low-Power Energy-Based Spike Detector ASIC for Implantable Multichannel BMIs," Electronics, vol. 11, no. 18, p. 2943, Sep. 2022, doi: 10.3390/electronics11182943.

6.j - G. Di Meo, **G. Saggese**, A. G. M. Strollo and D. De Caro, " MAC unit using Static Segmentation", **submitted** to IEEE Transactions on Emerging Topics in Computing.

7.j - I. Nunziata, E. Zacharelos**, G. Saggese**, A. M. G. Strollo and E. Napoli, " Approximate Squaring circuits exploiting Recursive Architectures" **submitted** to Integration Elsevier Journal.

Conference contributions:

1.c - I. Nunziata, E. Zacharelos**, G. Saggese**, A. M. G. Strollo and E. Napoli, "Approximate Recursive Multipliers Using Carry Truncation and Error Compensation," 2022 17th Conference on Ph.D Research in Microelectronics and Electronics (PRIME), 2022, pp. 137-140, doi: 10.1109/PRIME55000.2022.9816787.(**Golden Leaf award)**

2.c - **G. Saggese**, E. Zacharelos and A. G. M. Strollo, "Low Power Spike Detector for Brain-Silicon Interface using Differential Amplitude Slope Operator," 2022 17th Conference on Ph.D Research in Microelectronics and Electronics (PRIME), 2022, pp. 301-304, doi: 10.1109/PRIME55000.2022.9816758.

5. Conferences and seminars attended

- **G. Saggese**, E. Zacharelos and A. G. M. Strollo, "Low Power Spike Detector for Brain-Silicon Interface using Differential Amplitude Slope Operator," 2022 17th Conference on Ph.D Research in Microelectronics and Electronics ,PRIME2022-Villasimius,Italy, 12-15 June 2022 **(paper presented)**
- **G. Saggese** and A.G.M Strollo, "Low-Power Energy-Based Spike Detector for Brain-Silicon Interface" 53rd Annual Meeting of the Associazione Società Italiana di Elettronica (SIE), Pizzo (VV), Italy, 7-9 September 2022 (**poster presented**).
- Europractice Online Training Course "Comprehensive Digital IC Implementation & Sign-Off". 3/10/22-7/10/22.

6. Periods abroad and/or in international research institutions

None

7. Tutorship

Co-supervision of BSc thesis (Esposito Carmine) titled "Progettazione e realizzazione Hardware di un rilevatore di complessi QRS basato sull'operatore non lineare MOBD"

Co-supervision of BSc thesis (Tavassi Ciro) titled "Progettazione e realizzazione hardware di un rivelatore di complessi QRS basato sull'operatore non-lineare ASO".

Co-supervision of BSc thesis (Vaccaro Michele) titled “Studio di un sensore IoT basato su misure optofluidiche”.

8. Plan for year three

- **Research period abroad** (approx. January-June 2022) at the University of Applied Sciences of Fulda, Germany under the supervision of Prof. Martin Kumm Full Professor, Faculty of Applied Computer Science, Embedded Systems.
  Research Topics related to the approximate multipliers and arithmetic units for FPGA-optimized neural networks and compressor tree for FPGs.
- A first SoC based 256-channels spike detector prototype was designed, targeting the SoC Xilinx Zedboard, which includes an AFE interface, signal processing block, and the MCU Zynq-7000 to communicate with the host pc by TCP/IP protocol. **Ready to be connected and tested with the Brain28nm-ADCs chip.**
- The thesis topic will cover the analysis, design and comparison of several spikes detectors together with the integration of approximate computing arithmetic units to achieve ultra-low power and small silicon consumptions.