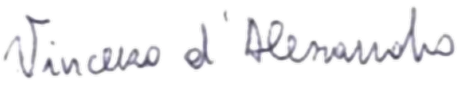
PhD in Information Technology and Electrical Engineering
Università degli Studi di Napoli Federico II

PhD Student: Giorgio Eliseo

Cycle: XL

Training and Research Activities Report

Year: First

Tutor: prof. Vincenzo d'Alessandro 

Co-Tutor:

Date: October 23 2026

Training and Research Activities Report

PhD in Information Technology and Electrical Engineering

Cycle: **Author:**

1. Information:

- **PhD student: Giorgio Eliseo**
- **DR number: DR999875**
- **Date of birth: October 1st 2000**
- **Master Science degree: Ingegneria Elettronica M61 University: Federico II**
- **Doctoral Cycle: XL**
- **Scholarship type: PNRR**
- **Tutor: Vincenzo d'Alessandro**
- **Co-tutor:**

2. Study and training activities:

Activity	Type[1]	Hours	Credits	Dates	Organizer	Certificate[2]
Solid State Transformers: fundamentals, insights, and new trends,	Seminar	2	0,4	20-12-2024	Andrea Cervone,	Y
How to boost your PhD	Course	14	5	(08-15-22-29/01/2025 05-12/02/2025)	Antigone Marino DIETI	Y
Scuola Nazionale per Dottorandi "F. Gasparini". XXVII Stage, Napoli: "Il computer quantistico a piattaforma superconduttiva a Federico II e il suo ecosistema"Imprenditorialità e proprietà intellettuale	Seminar	3	0.6	06/02/2025	F. Tafuri F. Farroni, L. Rossi, F. Dughiero, S. Leva	Y
Methodologies and Tools for conducting Systematic Literature Reviews and Systematic Mapping Studies – Prof. Domenico Amalfitano	Course	14	3	28-29/04/2025 - 05-06-09-12-14/05/2025	DIETI	Y
On the security of semantic watermarking to	seminar	1	0.2	29-04-2025	Dr. Erwin Quiring, DIETI	Y

detect AI-generated content.						
Fundamentals of Thermal and Thermomechanical Modeling for Electronics Reliability,	**Course**	**8**	**2**	**25-09-2025**	**Prof. Vincenzo d'Alessandro, Wendy Luiten and John H. J. Janssen THERMINIC**	**Y**

1) Courses, Seminar, Doctoral School, Research, Tutorship
2) Choose: Y or N

2.1. Study and training activities - credits earned

	Courses	Seminars	Research	Tutorship	Total
Bimonth 1	**0**	**0.4**	**9.6**	**0**	**10**
Bimonth 2	**5**	**0.6**	**4.4**	**0**	**10**
Bimonth 3	**0**	**0.2**	**9.8**	**0**	**10**
Bimonth 4	**3**	**0**	**7**	**0**	**10**
Bimonth 5	**0**	**0**	**10**	**0**	**10**
Bimonth 6	**2**	**0**	**8**	**0**	**10**
Total	**10**	**1.2**	**48.8**	**0**	**60**
Expected	**30 - 70**	**10 - 30**	**80 - 140**	**0 – 4.8**	

3. Research activity:

The accurate estimation of the junction temperature of an electronic device is a crucial part of the design process, as it is practically difficult or even impossible to directly measure the temperature reached within the internal layers of the device. Furthermore, simulations help reduce the costly and lengthy prototyping stages. To avoid the complexity of a TCAD FEM solver, circuit-based electrothermal simulations represent a viable alternative, offering a good trade-off between complexity and accuracy.

The methodology consists of a pre-processing stage, where a Thermal-Feedback-Block (TFB) is extracted by fitting data from FEM simulations or experimental campaigns. The TFB is described in a netlist compatible with any SPICE-like simulator, which associates temperature increments with the power dissipated by the circuit. Once the TFB accuracy is assessed, it can be included in an electrical schematic to simulate the electrothermal feedback in realistic scenarios.

The research carried out this year assessed the accuracy of TFBs extracted with the innovative VOLTERRA code, which generates accurate nonlinear thermal feedback blocks using a model order reduction approach, ensuring FEM-level accuracy with reduced computational times.

In parallel, last-generation low-voltage regulators for AI microprocessors have been studied, focusing specifically on vertical diffused trench field plate MOSFETs. These devices enable higher breakdown voltages and lower on-resistances thanks to a double buried field plate, referred to as the shield field plate, which enables the RESURF effect. However, these devices suffer from a pronounced spurious turn-on phenomenon, which is further aggravated by the temperature-dependent decrease in threshold voltage.

A first electrical characterization of a lumped PSPICE model has been conducted to accurately replicate reference waveforms. Further goals include presenting a parametric analysis of the switching energy required in DC-DC buck converters based on trench field plate VDMOS technology.

4. Research products:

1) Authors: Giorgio Eliseo, Vincenzo d'Alessandro, Lorenzo Codecasa, Antonio Pio Catalano, Ciro Scognamillo
Conference: 31st International Workshop on Thermal Investigations of ICs and Systems
Acronym: THERMINIC 2025
Title: VOLTERRA: An Innovative Approach for Accurate Nonlinear Thermal Modeling of Electronic Components
Status: Presented; accepted for publication
Year: 2025
Indexing: The publication will be submitted for inclusion in IEEE Xplore. IEEE Xplore is indexed in Scopus and ISI Web of Science.

5. Conferences and seminars attended

Conference Name: Thermal Investigations of ICs and Systems
Acronym: THERMINIC 2025
Location: Naples, Italy
Dates: September 24–26, 2025
Contribution: Presented a paper titled " VOLTERRA: An Innovative Approach for Accurate Nonlinear Thermal Modeling of Electronic Components"

Short Course: Fundamentals of Thermal and Thermomechanical Modeling for Electronics Reliability
Instructors: Wendy Luiten and John H. J. Janssen
Location: Naples, Italy (as part of THERMINIC 2025)
Date: September 24, 2025
Participation: Attended as a participant

6. Activity abroad:

No activity abroad was carried out during the current year.

7. Activity in partner companies:

Starting from October 1st, 2025, I began a scientific collaboration with ON Semiconductor Italy, as part of a research initiative co-funded by the PNRR (National Recovery and Resilience Plan). This company is also industrial partner co-funding the PhD scholarship.
During the first month of collaboration, I carried out research activities at the company's laboratories in Milano, focusing on the electrical characterization of advanced power devices. Specifically, I worked on developing a SPICE model capable of accurately reproducing experimental waveforms, with the goal of creating a reliable simulation framework for electrothermal analysis under realistic operating conditions.

Hosting Company: ON Semiconductor Italy
Location: Milano, Italy
Period: October 2025 – March 2026
Months foreseen in agreement: 6

8. Tutorship

No tutorship was carried out during the current year.